1.5MHz, 1A Synchronous Buck Regulator

## Features

- **1A Output Current**
- **Wide 2.7V~5.5V Input Voltage**
- **Fixed 1.5MHz Switching Frequency**
- **Low Dropout Operating at 100% duty cycle**
- **Low 25μA Quiescent Current**
- **Integrate Synchronous Rectifier**
- **0.6V Low Reference Voltage**
- **<0.5μA Input Current during Shutdown**
- **Current-Mode Operation with Internal Compensation**
  - **Stable with Ceramic Output Capacitors**
  - **Fast Line Transient Response**
- **Over-Voltage Protection**
- **Under Voltage Protection**
- **Over-Temperature Protection with Hysteresis**
- **Available in a TSOT-23-6A Package**
- **Halogen and Lead Free Available (RoHS Compliant)**

## General Description

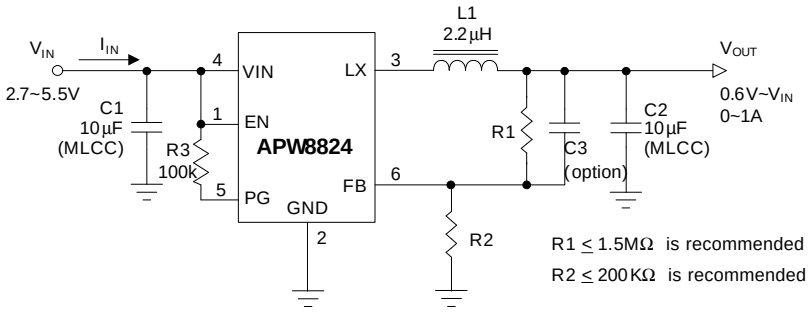
The APW8824 is a high efficiency monolithic synchronous buck regulator. APW8824 operates with a constant 1.5MHz switching frequency and using the inductor current as a controlled quantity in the current mode architecture. The 2.7V to 5.5V input voltage range makes the APW8824 ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable electrical devices. The internally fixed 1.5MHz operating frequency allows the use of small surface mount inductors and capacitors. The synchronous switches included inside increase the efficiency and eliminate the need for an external Schottky diode.

The APW8824 is available in TSOT-23-6A package

## Applications

- HD STB
- BT Mouse
- PND Instrument
- Portable Instrument

## Simplified Application Circuit



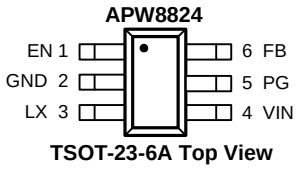

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

| | |
|---|---|
| APW8824 □□-□□□<br>Assembly Material<br>Handling Code<br>Temperature Range<br>Package Code | Package Code<br>CT : TSOT-23-6A<br>Operating Ambient Temperature Range<br>I : -40 to 85°C<br>Handling Code<br>TR : Tape & Reel<br>Assembly Material<br>G : Halogen and Lead Free Device |
| APW8824 CT: W24X X - Date Code | |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration




**TSOT-23-6A Top View**

## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Input Bias Supply Voltage (VIN to GND) | | -0.3 ~ 7 | V |
| | EN, FB, LX and PG to GND Voltage | | -0.3 ~ $V_{IN}$+0.3 | V |
| $V_{LX}$ | LX Voltage (LX to GND) | <30ns pulse width | -3 ~ 8 | V |
| | | >30ns pulse width | -0.3 ~ $V_{IN}$ +0.3 | |
| | Maximum Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature | | -65 ~ 150 | °C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature (10 Seconds) | | 260 | °C |

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Resistance in free air (Note 2) | 220 | °C/W |

Note 2: $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Bias Supply Voltage (VIN to GND) | 2.7 ~ 5.5 | V |
| $V_{OUT}$ | Converter Output Voltage | 0.6 ~ $V_{IN}$ | V |
| $I_{OUT}$ | Converter Output Current | 0 ~ 1 | A |
| L1 | Converter Output Inductor | 1.0 ~ 10 | µH |
| $C_{IN}$ | Converter Input Capacitor | 10 ~ 100 | µF |
| $C_{OUT}$ | Converter Output Capacitor | 10 ~ 100 | µF |
| $T_A$ | Ambient Temperature | -40 ~ 85 | °C |
| $T_J$ | Junction Temperature | -40 ~ 125 | °C |

Note 3: Refer to the application circuit for further information

## Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}$=3.6V and $T_A$= -40 ~ 85 °C. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8824 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | |
| $V_{IN}$ | Input Voltage Range | | 2.7 | - | 5.5 | V |
| $I_{DD}$ | Quiescent Current | $V_{FB}$ = 0.66V | - | 25 | 40 | µA |
| $I_{SD}$ | Shutdown Input Current | EN = GND | - | - | 0.5 | µA |
| **POWER-ON-RESET (POR) and LOCKOUT VOLTAGE THRESHOLDS** | | | | | | |
| | UVLO Threshold | | 2.1 | 2.35 | 2.6 | V |
| | UVLO Hysteresis | | - | 0.1 | - | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference Voltage | $T_A$ = 25 °C | 0.594 | 0.6 | 0.606 | V |
| | | $T_A$ = -40~85 °C, $T_J$ = -40~125 °C | 0.591 | - | 0.609 | V |
| | Output Voltage Accuracy | 0A < $I_{OUT}$ < 1A, $V_{IN}$ > 3.6V, $T_J$ =25 °C | -1.5 | - | +1.5 | % |
| $I_{FB}$ | FB Input Current | | -50 | - | 50 | nA |
| **INTERNAL POWER MOSFETS** | | | | | | |
| $F_{SW}$ | Switching Frequency | $V_{FB}$ = 0.6V | 1.2 | 1.5 | 1.8 | MHz |
| $R_{P-FET}$ | Main Switch ON Resistance | $I_{LX}$=200mA | - | 0.28 | 0.35 | Ω |
| $R_{N-FET}$ | Synchronous Switch ON Resistance | $I_{LX}$=200mA | - | 0.25 | 0.32 | Ω |
| | N-FET Switch Leakage Current | $V_{RUN}$ = GND, $V_{LX}$ = 5V | -0.1 | - | 0.1 | µA |
| | P-FET Switch Leakage Current | $V_{RUN}$ = GND, $V_{LX}$ = 0V | -0.1 | - | 0.1 | µA |

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## Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}$=3.6V and $T_A$= -40 ~ 85 °C. Typical values are at $T_A$=25°C.

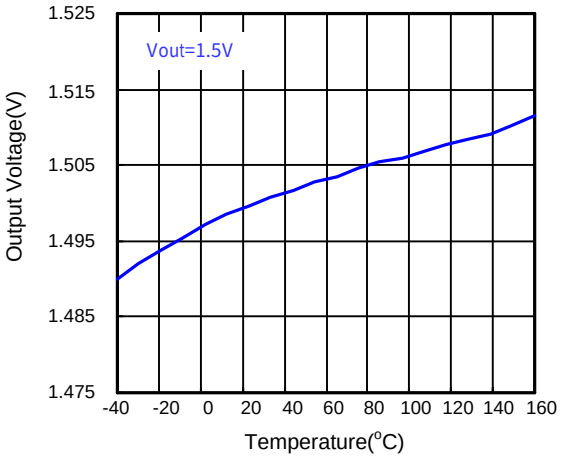
| Symbol | Parameter | Test Conditions | APW8824 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **INTERNAL POWER MOSFETS** | | | | | | |
| | Dead-time | (Note 4) | - | 5 | - | ns |
| | Duty Cycle | | 0 | - | 100 | % |
| **PROTECTION** | | | | | | |
| $I_{LIM}$ | Maximum Inductor Current Limit | $I_{P-FET}$, 2.7V≦$V_{IN}$≦6V | 2 | 2.5 | 3 | A |
| | N-FET Negative Current Limit | | - | 1 | - | A |
| $V_{OVP}$ | Over Voltage Protection Threshold | | 115 | 120 | 125 | %$V_{REF}$ |
| | OVP Debounce Time | | - | 20 | - | µs |
| $V_{UVP}$ | Under Voltage Protection Threshold | | 57 | 66 | 75 | %$V_{REF}$ |
| | UVP Debounce Time | | - | 15 | - | µs |
| | PG Threshold | PG in from Lower (PG Goes High) | 87 | 90 | 93 | %$V_{REF}$ |
| | | PG Low Hysteresis (PG Goes Low) | - | 3 | - | %$V_{REF}$ |
| | | PG in from Higher (PG Goes High) | 115 | 120 | 125 | %$V_{REF}$ |
| | | PG High Hysteresis (PG Goes Low) | - | 3 | - | %$V_{REF}$ |
| | PG High to Low debounce time ($V_{OUT}$ under shoot) | | - | 60 | - | µs |
| | PG High to Low debounce time ($V_{OUT}$ over shoot) | | - | 80 | - | µs |
| $T_{OTP}$ | Over-Temperature Protection | $T_J$ Rising | - | 150 | - | °C |
| **START-UP AND SHUTDOWN** | | | | | | |
| $T_{SS}$ | Soft-start Duration | (Note 4) | - | 0.7 | - | ms |
| | EN Input High Threshold | $V_{IN}$ = 2.7V~5.5V | - | - | 1.5 | V |
| | EN Input Low Threshold | $V_{IN}$ = 2.7V~5.5V | 0.4 | - | - | V |
| | EN Leakage Current | $V_{EN}$ = 5V, $V_{IN}$ = 5V | -1 | - | 1 | µA |
| | Power Good Pull Low Resistance | | - | 200 | - | Ω |

Note 4: Guaranteed by design, not production tested.

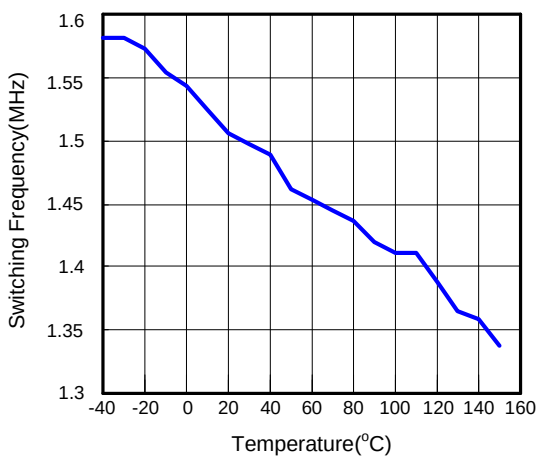
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## Typical Operating Characteristics

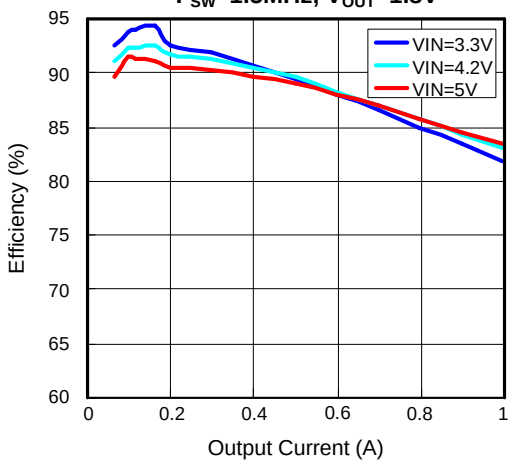
**Output Voltage vs. Temperature**



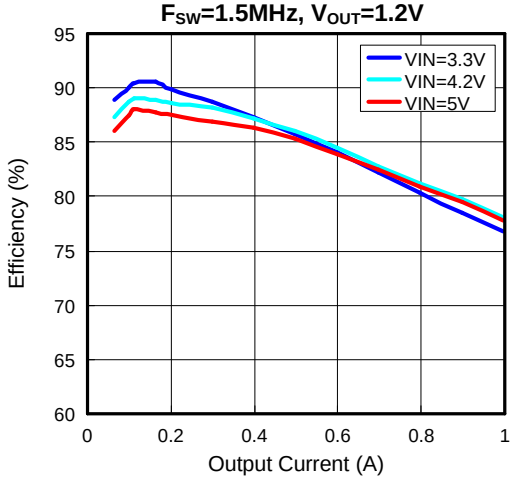

**Switching Frequency vs Temperature**




**Efficiency vs. Load Current**
**$F_{SW}$=1.5MHz, $V_{OUT}$=1.8V**



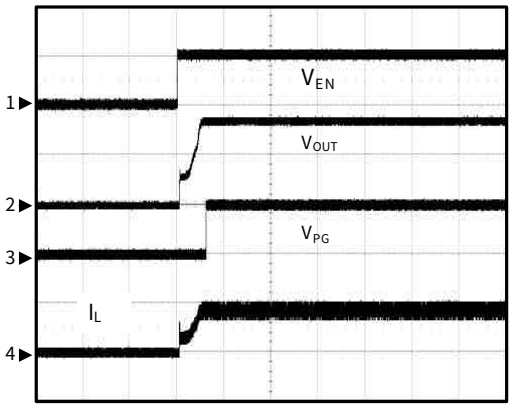

**Efficiency vs. Load Current**
**$F_{SW}$=1.5MHz, $V_{OUT}$=1.2V**



## Operating Waveforms

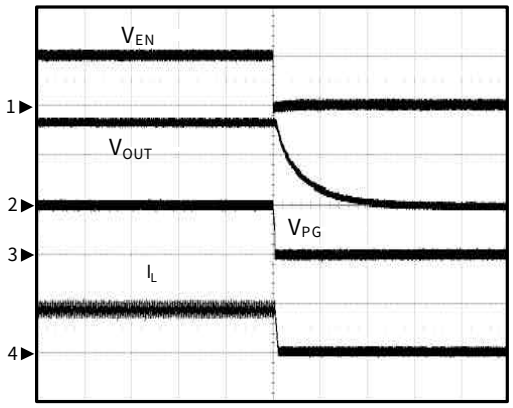
Refer to the typical application circuit. The test condition is $V_{IN}$=5V, $T_A$= 25°C unless otherwise specified.

**Enable**



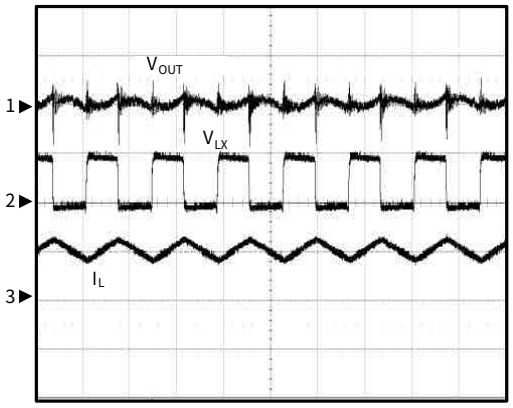

CH1:$V_{EN}$ , 5V/Div
CH2:$V_{OUT}$ , 1V/Div
CH3:$V_{PG}$ , 5V/Div
CH3:$I_L$ , 1A/Div
TIME: 1ms/Div

**Shutdown**



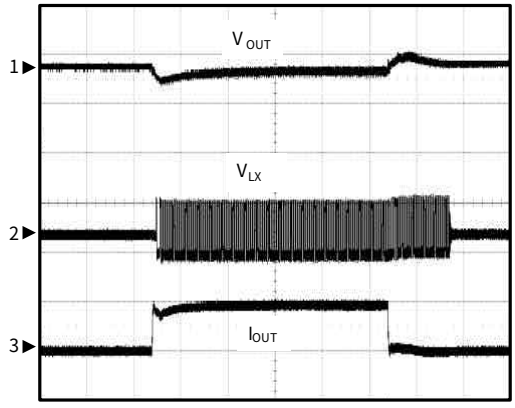

CH1: $V_{EN}$, 5V/Div
CH2: $V_{OUT,}$ 1V/Div
CH3: $V_{PG}$ 5V/Div
CH4: $I_L$, 1A/Div
TIME: 20µs/Div

**Output Ripple**




CH1: $V_{OUT}$, 20mV/Div,AC
CH2: $V_{LX}$ , 5V/Div
CH3: $I_L$ , 1A/Div
TIME: 20µs/Div

**Load Transient**



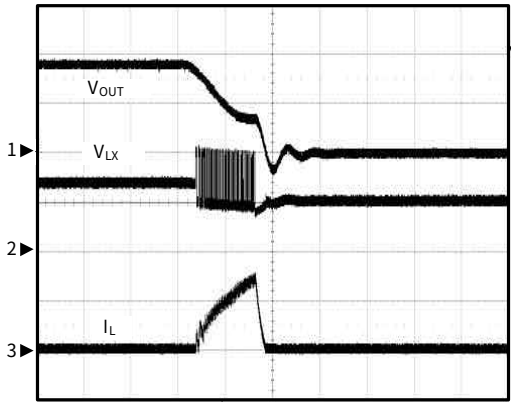

CH1: $V_{OUT}$, 100mV/Div,AC
CH2: $V_{LX}$,5V/Div
CH3: $I_{OUT}$ ,1A/Div
TIME: 100µs/Div

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## Operating Waveforms (Cont.)

Refer to the typical application circuit. The test condition is $V_{IN}$=5V, $T_A$= 25°C unless otherwise specified.

**Short Circuit Protection**

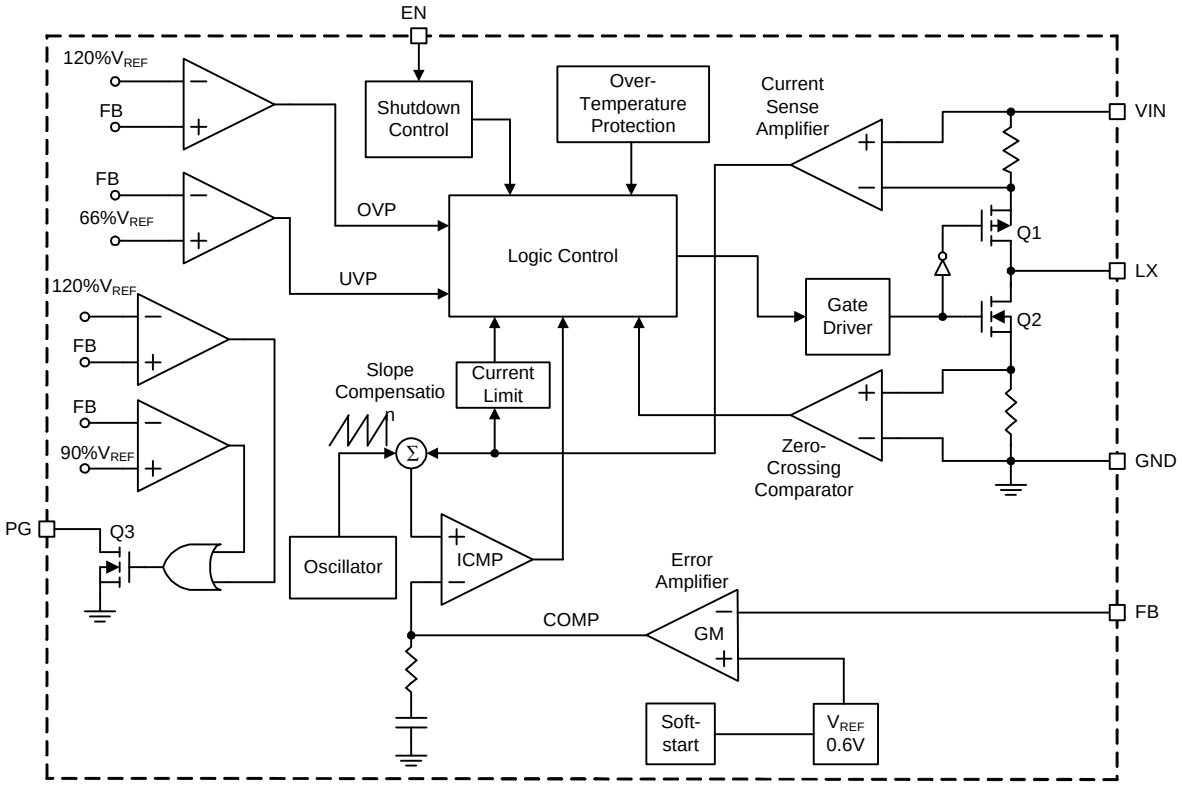



CH1: $V_{OUT}$, 1V/Div
CH2: $V_{LX}$, 5V/Div
CH3: $I_L$, 2A/Div
TIME: 20μs/Div

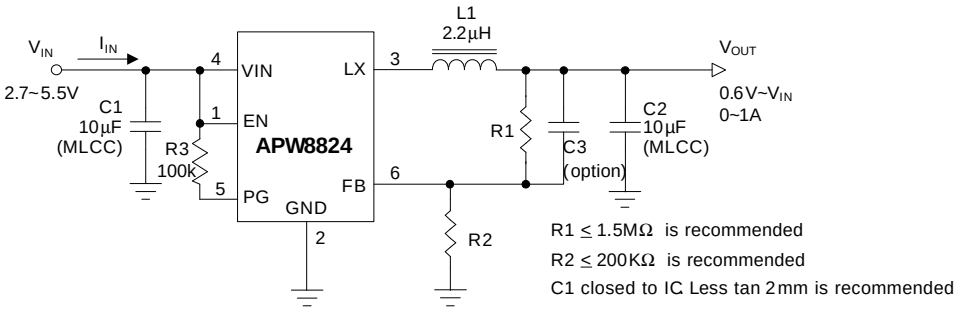
## Pin Description

| PIN | | Function |
|---|---|---|
| NO. | NAME | |
| 1 | EN | Enable Control Input. Forcing this pin above 1.5V enables the device. Forcing this pin below 0.4V shuts it down. In shutdown, all functions are disabled to decrease the supply current below 0.5μA. **Do not leave EN pin floating.** |
| 2 | GND | Power and Signal Ground. |
| 3 | LX | Switch Node Connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFETs switches. |
| 4 | VIN | Device and Converter Supply Pin. Must be closely decoupled to GND with a 10μF or greater ceramic capacitor. |
| 5 | PG | Power Good Output. This pin is open-drain logic output that is pulled to ground when the output voltage is not within 10%of regulation point. |
| 6 | FB | Feedback Input Pin. The buck regulator senses feedback voltage via FB and regulates the FB voltage at 0.6V. Connecting FB with a resistor-divider from the output sets the output voltage of the buck converter. |

## Block Diagram



## Typical Application Circuits



## Function Description

### Main Control Loop

The APW8824 is a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal P-channel power MOSFET is turned on each cycle. The peak inductor current which ICMP turn off the P-FET is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external resistive divider connected between VOUT and ground allows the EAMP to receive an output feedback voltage VFB at FB pin. When the load current increases, it causes a slightly decrease in VFB relative to the 0.6V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

### Under-Voltage Lockout

An under-voltage lockout function prevents the device from operating if the input voltage on VIN is lower than approximately 2.35V. The device automatically enters the shutdown mode if the voltage on VIN drops below approximately 2.35V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter.

### Soft-start

The APW8824 has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage (0.6V typical) until the ramp voltage reaches the reference voltage. Then the voltage on FB regulated at reference voltage.

### Enable/Shutdown

Driving EN to ground places the APW8824 in shutdown mode. When in shutdown, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to 0.5μA maximum.

### Pulse Frequency Modulation Mode (PFM)

The APW8824 is a fixed frequency PWM peak current mode control step-down converter. At light loads, the APW8824 will automatically enter in pulse frequency mode operation to reduce the dominant switching losses. In PFM operation, the inductor current may reach zero or reverse on each pulse. A zero current comparator turn off the N-FET, forcing DCM operation at light load. These controls get very low quiescent current, help to maintain high efficiency over the complete load range.

### Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the APW8824 uses a special scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

### Dropout Operation

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will be determined by the input voltage minus the voltage drop across the P-FET and the inductor.

An important detail to remember is that on resistance of P-FET switch will increase at low input supply voltage. Therefore, the user should calculate the power dissipation when the APW8824 is used at 100% duty cycle with low input voltage.

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## Function Description

**Over-Temperature Protection (OTP)**

The over-temperature circuit limits the junction temperature of the APW8824. When the junction temperature exceeds 150°C, a thermal sensor turns off the both power MOSFETs. It is a latch protection.

**Over Voltage Protection**

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 120% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will turn on low side N-MOSFET and shutdown the converter output.

**Output Under Voltage Protection**

In the operational process, if a short circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold.

The under-voltage threshold is 66% of the nominal output voltage. The under-voltage comparator has a built-in 15μs noise filter to prevent the chips from wrong UVP shutdown being caused by noise. APW8824 will be latched after under-voltage protection.

**Power Good**

PG is actively held low in shutdown and soft-start status. In the soft-start process, the PG is an open-drain. When the soft-start is finished, the PG is released. In normal operation, the PG window is from 90% to 120% of the converter reference voltage. When the output voltage has to stay within this window, PG signal will become high. When the output voltage outruns 90% or 120% of the target voltage, PG signal will be pulled low immediately.

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## Application Information

### Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 10μF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

### Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, $\Delta I_L$, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

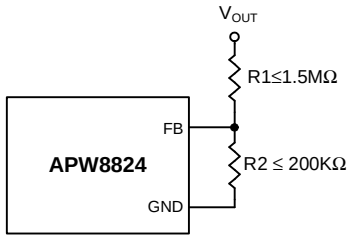
$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

### Output Voltage Setting

The output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 200kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 0.6\cdot\left(1+\frac{R1}{R2}\right)$$




### Output Capacitor Selection

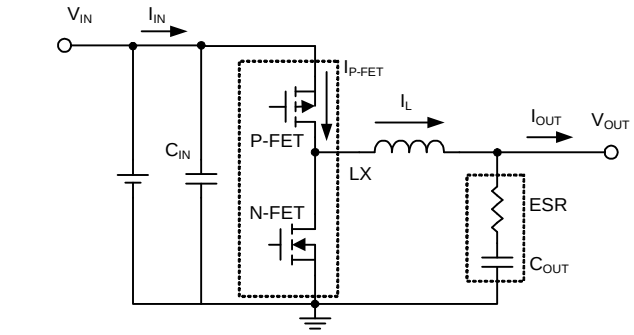
The current-mode control scheme of the APW8824 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

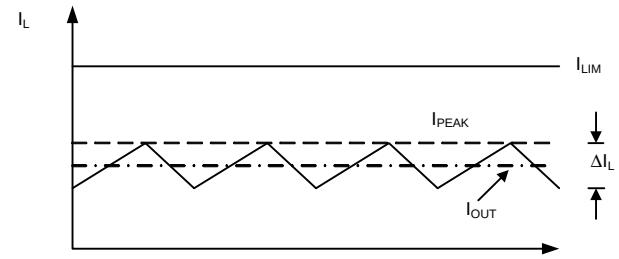
$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

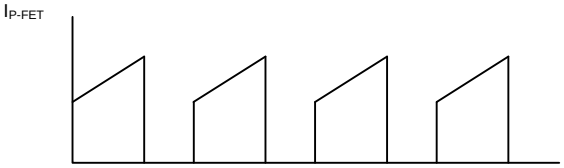
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

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## Application Information (Cont.)




**Thermal Considerations**

In most applications the APW8824 does not dissipate much heat due to its high efficiency. But, in applications where the APW8824 is running at high ambient temperature with low supply voltage and high duty cycles, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the LX node will become high impedance.

To avoid the APW8824 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The power dissipated by the part is approximated:

$$P_D \cong I_{OUT}^2 \times (R_{P-FET} \times D + R_{N-FET} \times (1-D))$$

The temperature rise is given by:

$$TR = (P_D)(\theta_{JA})$$

Where PD is the power dissipated by the regulator, D is duty cycle of main switch

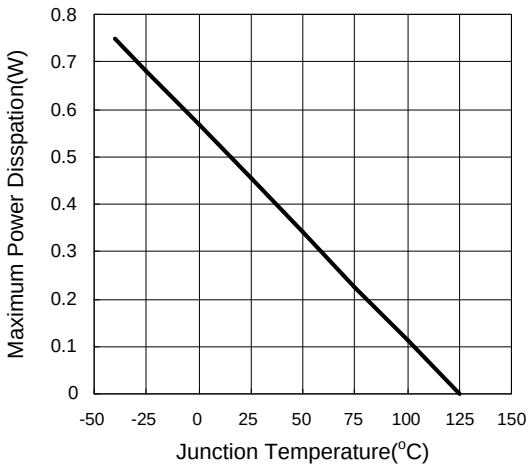
$$D = V_{OUT}/V_{IN}$$

The $\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, $T_J$, is given by:

$$T_J = T_A + T_R$$

Where $T_A$ is the ambient temperature.

The maximum power dissipation on the device can be shown as follow figure:



## Application Information (Cont.)

**Layout Considerations**

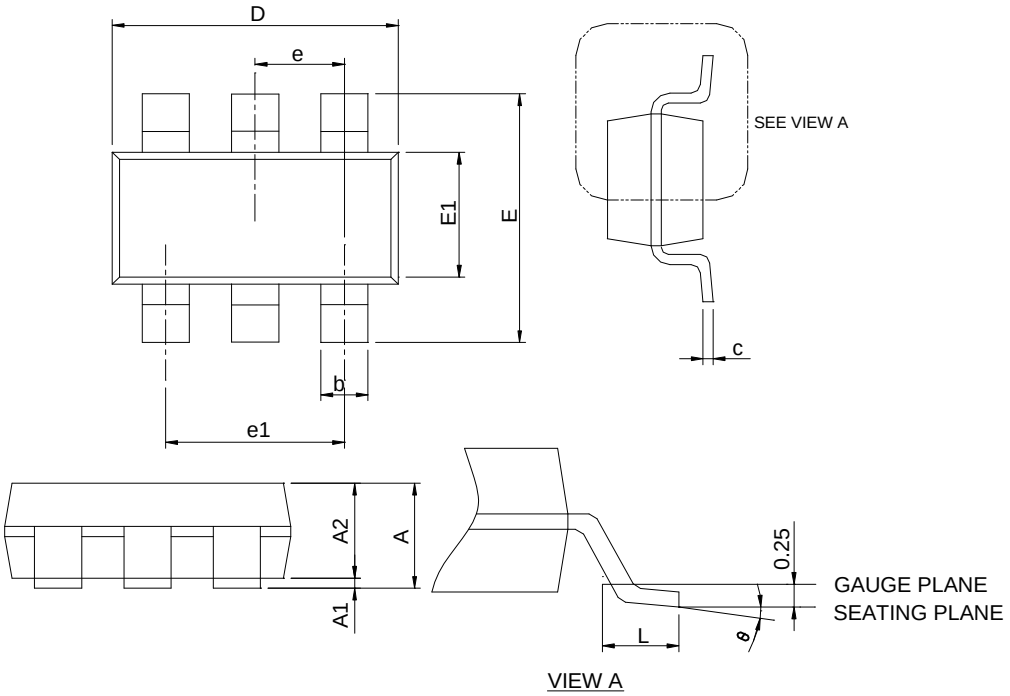
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

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## Package Information

**TSOT-23-6A**

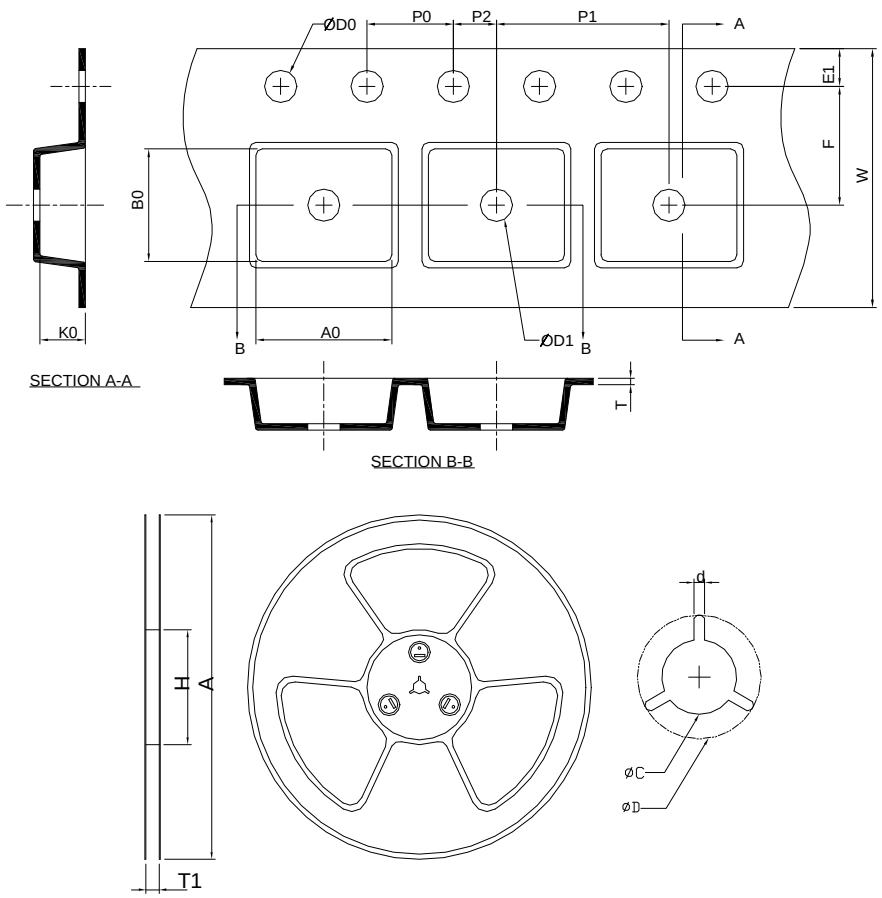



| SYMBOL | TSOT-23-6A | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 1.00 | 0.028 | 0.039 |
| A1 | 0.01 | 0.10 | 0.000 | 0.004 |
| A2 | 0.70 | 0.90 | 0.028 | 0.035 |
| b | 0.30 | 0.50 | 0.012 | 0.020 |
| c | 0.08 | 0.20 | 0.003 | 0.008 |
| D | 2.70 | 3.10 | 0.106 | 0.122 |
| E | 2.60 | 3.00 | 0.102 | 0.118 |
| E1 | 1.40 | 1.80 | 0.055 | 0.071 |
| e | 0.95 BSC | | 0.037 BSC | |
| e1 | 1.90 BSC | | 0.075 BSC | |
| L | 0.30 | 0.60 | 0.012 | 0.024 |
| θ | $0^o$ | $8^o$ | $0^o$ | $8^o$ |

Note : 1. Followed from JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

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## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TSOT-23-6A | 178.0±2.00 | 50 MIN. | 8.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 8.0±0.30 | 1.75±0.10 | 3.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 4.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.0 MIN. | 0.6+0.00 -0.40 | 3.20±0.20 | 3.10±0.20 | 1.20±0.20 |

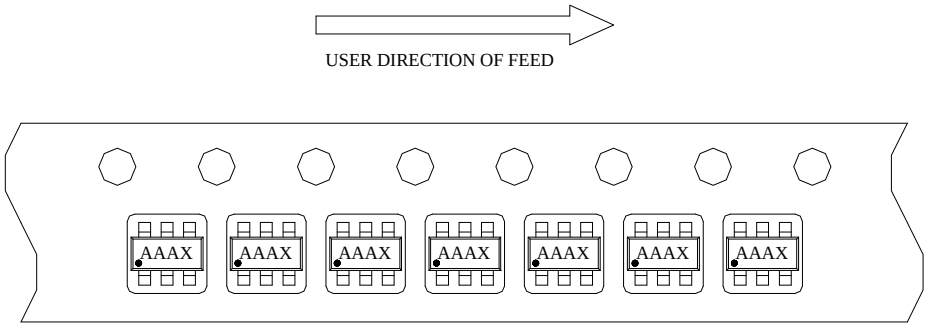
(mm)

## Devices Per Unit

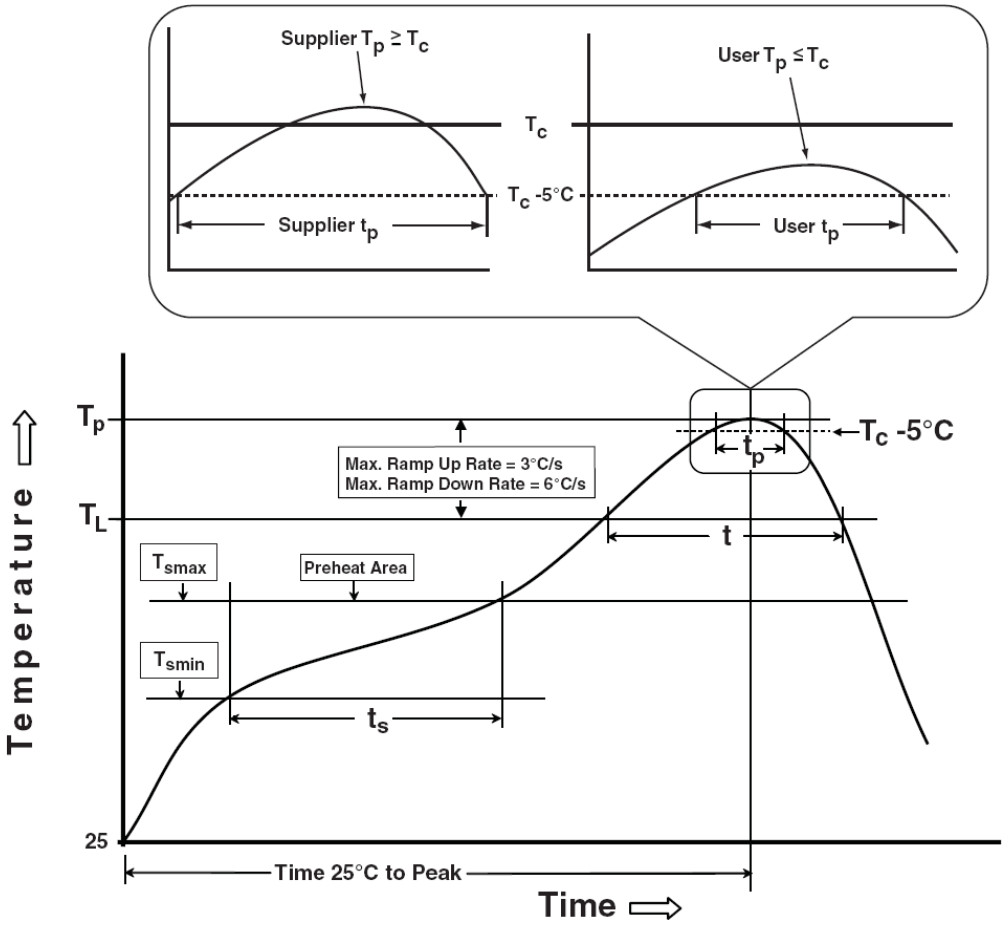
| Package Type | Unit | Quantity |
|---|---|---|
| **TSOT-23-6A** | Tape & Reel | 3000 |

## Taping Direction Information

**TSOT-23-6A**




## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ $^3$350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ Tj=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

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## Customer Service

**Anpec Electronics Corp.**
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838