PDTD113E series

NPN 500 mA, 50 V resistor-equipped transistors; R1 = 1 kΩ, R2 = 1 kΩ

Rev. 02 — 16 November 2009 Product data sheet

1. Product profile

1.1 General description

500 mA NPN Resistor-Equipped Transistors (RET) family.

Table 1. Product overview

Type number	Package			PNP complement
	NXP	JEITA	JEDEC	
PDTD113EK	SOT346	SC-59A	TO-236	PDTB113EK
PDTD113ES[1]	SOT54	SC-43A	TO-92	PDTB113ES
PDTD113ET	SOT23	-	TO-236AB	PDTB113ET

[1] Also available in SOT54A and SOT54 variant packages (see Section 2).

1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- 500 mA output current capability
- Reduces component count
- Reduces pick and place costs
- ±10 % resistor ratio tolerance

1.3 Applications

- Digital application in automotive and industrial segments
- Controlling IC inputs
- Cost saving alternative for BC817 series in digital applications
- Switching loads

1.4 Quick reference data

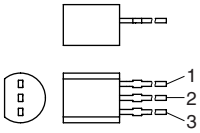
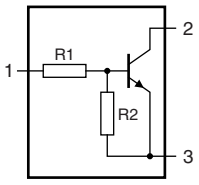
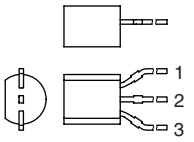
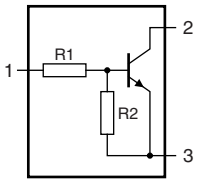
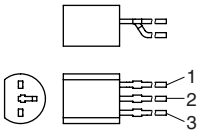
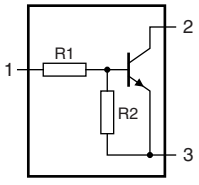
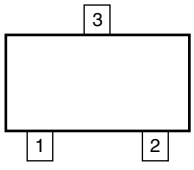
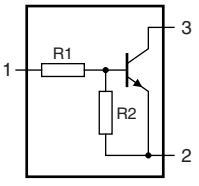
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current (DC)		-	-	500	mA
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.9	1.0	1.1	

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2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
SOT54			
1	input (base)	 001aab347	 006aaa145
2	output (collector)		
3	GND (emitter)		
SOT54A			
1	input (base)	 001aab348	 006aaa145
2	output (collector)		
3	GND (emitter)		
SOT54 variant			
1	input (base)	 001aab447	 006aaa145
2	output (collector)		
3	GND (emitter)		
SOT23, SOT346			
1	input (base)	 006aaa144	 sym007
2	GND (emitter)		
3	output (collector)		

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3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTD113EK	SC-59A	plastic surface mounted package; 3 leads	SOT346
PDTD113ES[1]	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTD113ET	-	plastic surface mounted package; 3 leads	SOT23

[1] Also available in SOT54A and SOT54 variant packages (see Section 2 and Section 9).

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PDTD113EK	E1
PDTD113ES	D113ES
PDTD113ET	*7R

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	10	V
V_I	input voltage				
	positive		-	+10	V
	negative		-	−10	V
I_O	output current (DC)		-	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C [1]			
	SOT346		-	250	mW
	SOT54		-	500	mW
	SOT23		-	250	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		−65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]				
	SOT346			-	-	500	K/W
	SOT54			-	-	250	K/W
	SOT23			-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

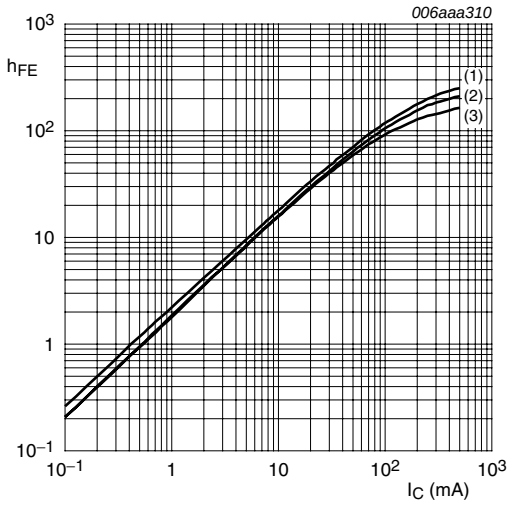
7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = 40 V; I_E = 0 A	-	-	100	nA
		V_{CB} = 50 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 50 V; I_B = 0 A	-	-	0.5	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	4	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 50 mA	33	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 50 mA; I_B = 2.5 mA	-	-	0.3	V
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 μA	0.6	1.1	1.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 20 mA	1.0	1.4	1.8	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.9	1	1.1	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 100 MHz	-	7	-	pF

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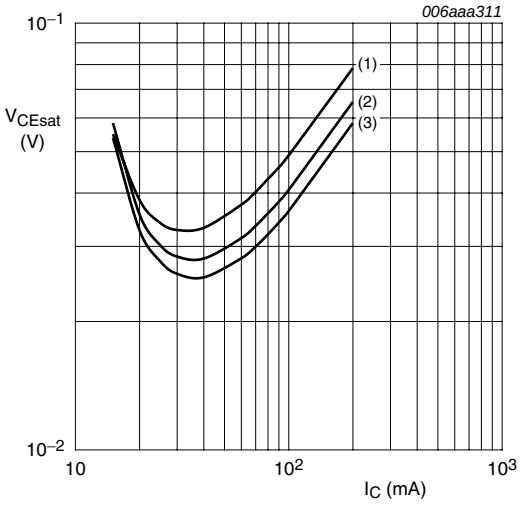
V_{CE} = 5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 1. DC current gain as a function of collector current; typical values



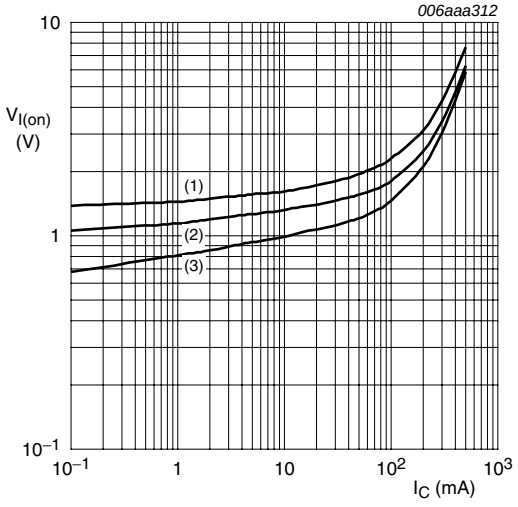
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values



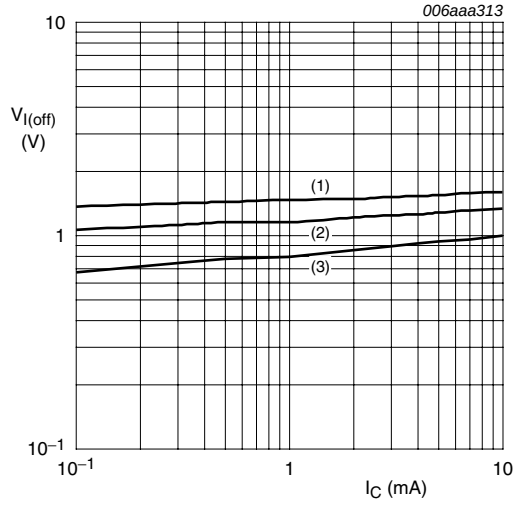
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 3. On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 4. Off-state input voltage as a function of collector current; typical values

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8. Package outline

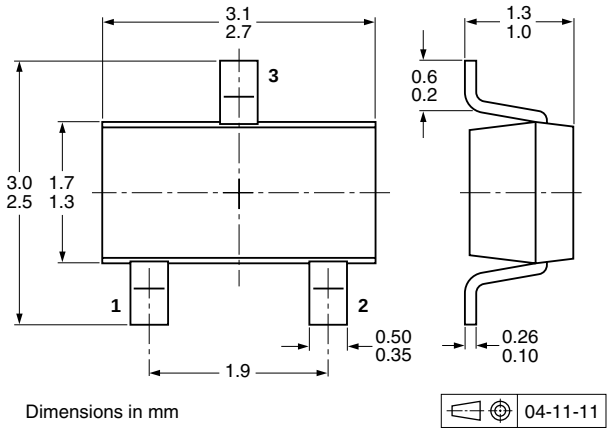


Fig 5. Package outline SOT346 (SC-59A/TO-236)

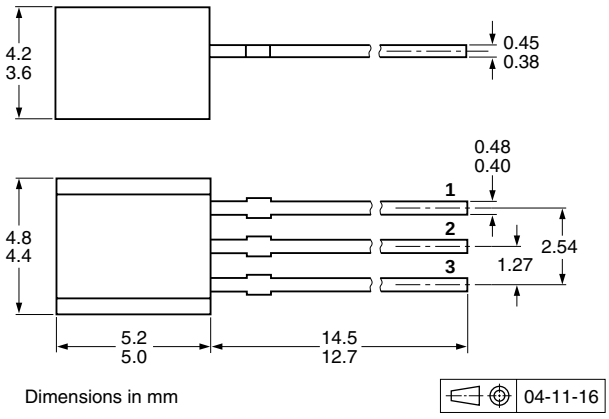


Fig 6. Package outline SOT54 (SC-43A/TO-92)

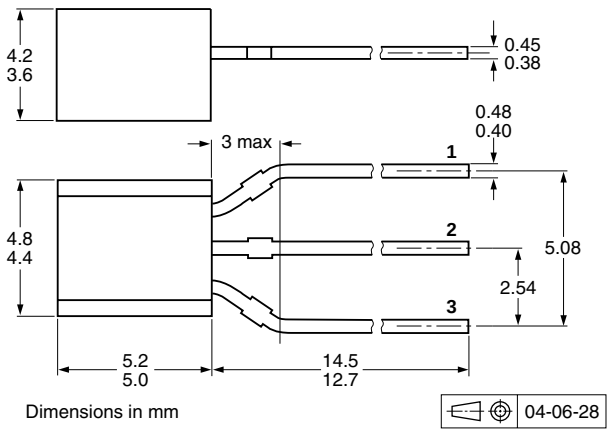


Fig 7. Package outline SOT54A

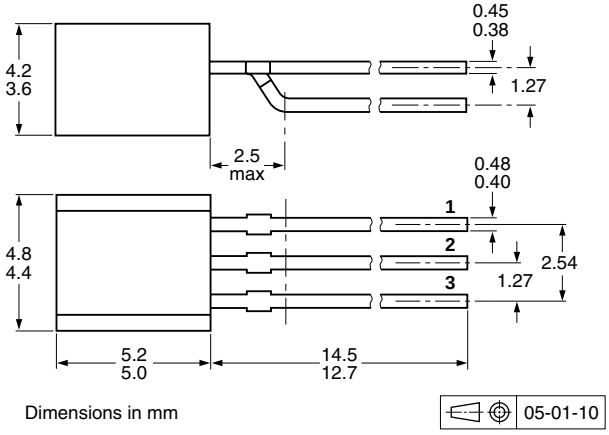


Fig 8. Package outline SOT54 variant

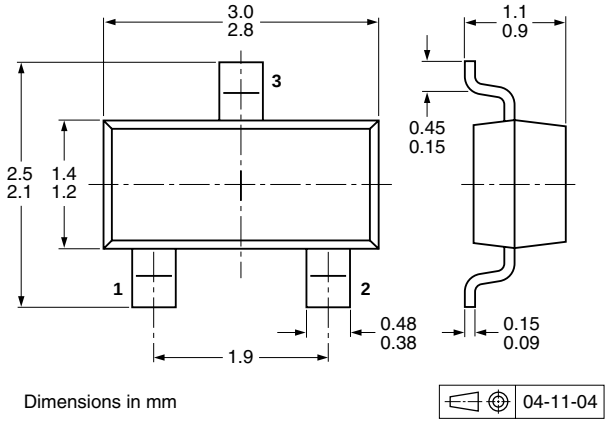


Fig 9. Package outline SOT23 (TO-236AB)

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9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTD113EK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTD113ES	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
		tape ammopack, wide pitch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PDTD113ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235

[1] For further information and the availability of packing methods, see Section 12.

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10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTD113E_SER_2	20091116	Product data sheet	-	PDTD113E_SER_1
Modifications:	• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.			
PDTD113E_SER_1	20050414	Product data sheet	-	-

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11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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