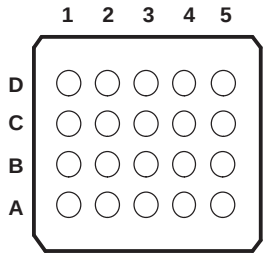
# TXB0108
# 8-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTO-DIRECTION SENSING AND ±15-kV ESD PROTECTION

SCES643A – NOVEMBER 2006 – REVISED JANUARY 2007

## FEATURES

- **1.2 V to 3.6 V on A Port and 1.65 to 5.5 V on B Port ($V_{CCA} \leq V_{CCB}$)**
- **$V_{CC}$ Isolation Feature – If Either $V_{CC}$ Input Is at GND, All Outputs Are in the High-Impedance State**
- **OE Input Circuit Referenced to $V_{CCA}$**
- **Low Power Consumption, 4-μA Max $I_{CC}$**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **A Port**
    - **2000-V Human-Body Model (A114-B)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**
  - **B Port**
    - **±15-kV Human-Body Model (A114-B)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**

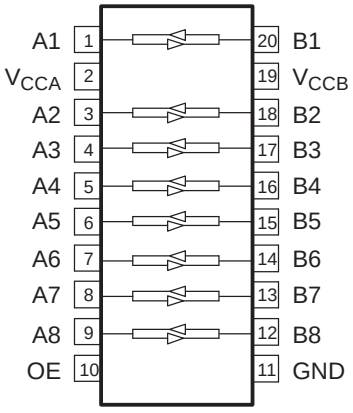
**GXY OR ZXY PACKAGE**
**(BOTTOM VIEW)**



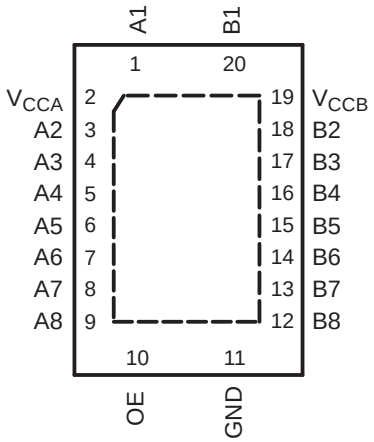

**TERMINAL ASSIGNMENTS**
**(20-Ball GXY/ZXY Package)**

| | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| **D** | $V_{CCB}$ | B2 | B4 | B6 | B8 |
| **C** | B1 | B3 | B5 | B7 | GND |
| **B** | A1 | A3 | A5 | A7 | OE |
| **A** | $V_{CCA}$ | A2 | A4 | A6 | A8 |

**PW PACKAGE**
**(TOP VIEW)**




**RGY PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

This 8-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track $V_{CCA}$. $V_{CCA}$ accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track $V_{CCB}$. $V_{CCB}$ accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. $V_{CCA}$ should not exceed $V_{CCB}$.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0101 is desinged so that the OE input circuit is supplied by $V_{CCA}$.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### ORDERING INFORMATION

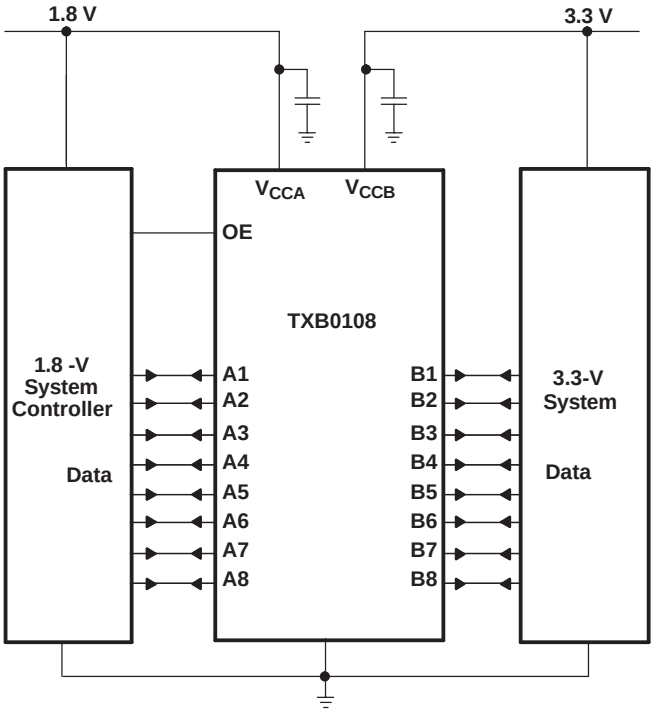
| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | TXB0108RGYR | YE08 |
| | TSSOP – PW | Reel of 2000 | TXB0108PWR | YE08 |
| | VFBGA – GXY | Reel of 2500 | TXB0108GXYR | YE08 |
| | VFBGA – ZXY (Pb-free) | Reel of 2500 | TXB0108ZXYR | YE08 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### PIN DESCRIPTION

| NO. | NAME | FUNCTION |
|---|---|---|
| 1 | A1 | Input/output 1. Referenced to $V_{CCA}$. |
| 2 | $V_{CCA}$ | A-port supply voltage. 1.1 V ≤ $V_{CCA}$ ≤ 3.6 V, $V_{CCA}$ ≤ $V_{CCB}$. |
| 3 | A2 | Input/output 2. Referenced to $V_{CCA}$. |
| 4 | A3 | Input/output 3. Referenced to $V_{CCA}$. |
| 5 | A4 | Input/output 4. Referenced to $V_{CCA}$. |
| 6 | A5 | Input/output 5. Referenced to $V_{CCA}$. |
| 7 | A6 | Input/output 6. Referenced to $V_{CCA}$. |
| 8 | A7 | Input/output 7. Referenced to $V_{CCA}$. |
| 9 | A8 | Input/output 8. Referenced to $V_{CCA}$. |
| 10 | OE | Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to $V_{CCA}$. |
| 11 | GND | Ground |
| 12 | B8 | Input/output 8. Referenced to $V_{CCB}$. |
| 13 | B7 | Input/output 7. Referenced to $V_{CCB}$. |
| 14 | B6 | Input/output 6. Referenced to $V_{CCB}$. |
| 15 | B5 | Input/output 5. Referenced to $V_{CCB}$. |
| 16 | B4 | Input/output 4. Referenced to $V_{CCB}$. |
| 17 | B3 | Input/output 3. Referenced to $V_{CCB}$. |
| 18 | B2 | Input/output 2. Referenced to $V_{CCB}$. |
| 19 | $V_{CCB}$ | B-port supply voltage. 1.65 V ≤ $V_{CCB}$ ≤ 5.5 V. |
| 20 | B1 | Input/output 1. Referenced to $V_{CCB}$. |

## TYPICAL OPERATING CIRCUIT




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage range | | –0.5 | 4.6 | V |
| $V_{CCB}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | A inputs | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | B inputs | –0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance | GXY/ZXY package(4) | | 78 | °C/W |
| | | PW package(4) | | 83 | |
| | | RGY package(5) | | 37 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CCA}$ and $V_{CCB}$ are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions[1][2]

| | | | $V_{CCA}$ | $V_{CCB}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | | 1.2 | 3.6 | V |
| $V_{CCB}$ | | | | | 1.65 | 5.5 | |
| $V_{IH}$ | High-level input voltage | Data inputs | 1.2 V to 3.6 V | 1.65 V to 5.5 V | $V_{CCI}$ x 0.65[3] | $V_{CCI}$ | V |
| | | OE | | | $V_{CCA}$ x 0.65 | 5.5 | |
| $V_{IL}$ | Low-level input voltage | Data inputs | 1.2 V to 5.5 V | 1.65 V to 5.5 V | 0 | $V_{CCI}$ x 0.35[3] | V |
| | | OE | 1.2 V to 3.6 V | | 0 | $V_{CCA}$ x 0.35 | |
| Δt/Δv | Input transition rise or fall rate | A-port inputs | 1.2 V to 3.6 V | 1.65 V to 5.5 V | | 40 | ns/V |
| | | B-port inputs | 1.2 V to 3.6 V | 1.65 V to 3.6 V | | 40 | |
| | | | | 4.5 V to 5.5 V | | 30 | |
| $T_A$ | Operating free-air temperature | | | | –40 | 85 | °C |

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at $V_{CCI}$ or both at GND.
(2) $V_{CCA}$ must be less than or equal to $V_{CCB}$ and must not exceed 3.6 V.
(3) $V_{CCI}$ is the supply voltage associated with the input port.

## Electrical Characteristics(1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | $T_A$ = 25°C | | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{OHA}$ | | $I_{OH}$ = –20 µA | 1.2 V | | | 1.1 | | | | V |
| | | | 1.4 V to 3.6 V | | | | | $V_{CCA}$ – 0.4 | | |
| $V_{OLA}$ | | $I_{OL}$ = 20 µA | 1.2 V | | | 0.9 | | | | V |
| | | | 1.4 V to 3.6 V | | | | | | 0.4 | |
| $V_{OHB}$ | | $I_{OH}$ = –20 µA | | 1.65 V to 5.5 V | | | | $V_{CCB}$ – 0.4 | | V |
| $V_{OLB}$ | | $I_{OL}$ = 20 µA | | 1.65 V to 5.5 V | | | | | 0.4 | V |
| $I_I$ | OE | | 1.2 V to 3.6 V | 1.65 V to 5.5 V | | | ±1 | | ±2 | µA |
| $I_{off}$ | A port | | 0 V | 0 V to 5.5 V | | | ±1 | | ±2 | µA |
| | B port | | 0 V to 3.6 V | 0 V | | | ±1 | | ±2 | |
| $I_{OZ}$ | A or B port | OE = GND | 1.2 V to 3.6 V | 1.65 V to 5.5 V | | | ±1 | | ±2 | µA |
| $I_{CCA}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2 V | 1.65 V to 5.5 V | | 0.06 | | | | µA |
| | | | 1.4 V to 3.6 V | | | | | | 5 | |
| | | | 3.6 V | 0 V | | | | | 2 | |
| | | | 0 V | 5.5 V | | | | | –2 | |
| $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2 V | 1.65 V to 5.5 V | | 3.4 | | | | µA |
| | | | 1.4 V to 3.6 V | | | | | | 5 | |
| | | | 3.6 V | 0 V | | | | | –2 | |
| | | | 0 V | 5.5 V | | | | | 2 | |
| $I_{CCA}$ + $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2 V | 1.65 V to 5.5 V | | 3.5 | | | | µA |
| | | | 1.4 V to 3.6 V | | | | | | 10 | |
| $I_{CCZA}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0, OE = GND | 1.2 V | 1.65 V to 5.5 V | | 0.05 | | | | µA |
| | | | 1.4 V to 3.6 V | | | | | | 5 | |
| $I_{CCZB}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0, OE = GND | 1.2 V | 1.65 V to 5.5 V | | 3.3 | | | | µA |
| | | | 1.4 V to 3.6 V | | | | | | 5 | |
| $C_I$ | OE | | 1.2 V to 3.6 V | 1.65 V to 5.5 V | | 5 | | | 5.5 | pF |
| $C_{io}$ | A port | | 1.2 V to 3.6 V | 1.65 V to 5.5 V | | 5 | | | 6.5 | pF |
| | B port | | | | | 8 | | | 10 | |

(1) $V_{CCI}$ is the supply voltage associated with the input port.
(2) $V_{CCO}$ is the supply voltage associated with the output port.

## Timing Requirements

$T_A$ = 25°C, $V_{CCA}$ = 1.2 V

| | | | $V_{CCB}$ = 1.8 V | $V_{CCB}$ = 2.5 V | $V_{CCB}$ = 3.3 V | $V_{CCB}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| | Data rate | | 20 | 20 | 20 | 20 | Mbps |
| $t_w$ | Pulse duration | Data inputs | 50 | 50 | 50 | 50 | ns |

## Timing Requirements

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 V ± 0.1 V (unless otherwise noted)

| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| | Data rate | | | 50 | | 50 | | 50 | | 50 | Mbps |
| $t_w$ | Pulse duration | Data inputs | 20 | | 20 | | 20 | | 20 | | ns |

## Timing Requirements

over recommended operating free-air temperature range, $V_{CCA}$ = 1.8 V ± 0.15 V (unless otherwise noted)

| | | | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| | Data rate | | | 52 | | 60 | | 60 | | 60 | Mbps |
| $t_w$ | Pulse duration | Data inputs | 19 | | 17 | | 17 | | 17 | | ns |

## Timing Requirements

over recommended operating free-air temperature range, $V_{CCA}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| | | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| | Data rate | | | 70 | | 100 | | 100 | Mbps |
| $t_w$ | Pulse duration | Data inputs | 14 | | 10 | | 10 | | ns |

## Timing Requirements

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | Data rate | | | 100 | | 100 | Mbps |
| $t_w$ | Pulse duration | Data inputs | 10 | | 10 | | ns |

## Switching Characteristics

$T_A$ = 25°C, $V_{CCA}$ = 1.2 V

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V | $V_{CCB}$ = 2.5 V | $V_{CCB}$ = 3.3 V | $V_{CCB}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $t_{pd}$ | A | B | 9.5 | 7.9 | 7.6 | 8.5 | ns |
| | B | A | 9.2 | 8.8 | 8.4 | 8 | |
| $t_{en}$ | OE | A | 1 | 1 | 1 | 1 | µs |
| | | B | 1 | 1 | 1 | 1 | |
| $t_{dis}$ | OE | A | 20 | 17 | 17 | 18 | ns |
| | | B | 20 | 16 | 15 | 15 | |
| $t_{rA}$, $t_{fA}$ | A-port rise and fall times | | 4.1 | 4.4 | 4.1 | 3.9 | ns |
| $t_{rB}$, $t_{fB}$ | B-port rise and fall times | | 5 | 5 | 5.1 | 5.1 | ns |
| $t_{SK(O)}$ | Channel-to-channel skew | | 2.4 | 1.7 | 1.9 | 7 | ns |
| Max data rate | | | 20 | 20 | 20 | 20 | Mbps |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 V ± 0.1 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.4 | 12.9 | 1.2 | 10.1 | 1.1 | 10 | 0.8 | 9.9 | ns |
| | B | A | 0.9 | 14.2 | 0.7 | 12 | 0.4 | 11.7 | 0.3 | 13.7 | |
| $t_{en}$ | OE | A | | 1 | | 1 | | 1 | | 1 | µs |
| | | B | | 1 | | 1 | | 1 | | 1 | |
| $t_{dis}$ | OE | A | 6.6 | 33 | 6.4 | 25.3 | 6.1 | 23.1 | 5.9 | 24.6 | ns |
| | | B | 6.6 | 35.6 | 5.8 | 25.6 | 5.5 | 22.1 | 5.6 | 20.6 | |
| $t_{rA}$, $t_{fA}$ | A-port rise and fall times | | 0.8 | 6.5 | 0.8 | 6.3 | 0.8 | 6.3 | 0.8 | 6.3 | ns |
| $t_{rB}$, $t_{fB}$ | B-port rise and fall times | | 1 | 7.3 | 0.7 | 4.9 | 0.7 | 4.6 | 0.6 | 4.6 | ns |
| $t_{SK(O)}$ | Channel-to-channel skew | | | 2.6 | | 1.9 | | 1.6 | | 1.3 | ns |
| Max data rate | | | 50 | | 50 | | 50 | | 50 | | Mbps |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 1.8 V ± 0.15 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.6 | 11 | 1.4 | 7.7 | 1.3 | 6.8 | 1.2 | 6.5 | ns |
| | B | A | 1.5 | 12 | 1.2 | 8.4 | 0.8 | 7.6 | 0.5 | 7.1 | |
| $t_{en}$ | OE | A | | 1 | | 1 | | 1 | | 1 | µs |
| | | B | | 1 | | 1 | | 1 | | 1 | |
| $t_{dis}$ | OE | A | 5.9 | 26.7 | 5.6 | 21.6 | 5.4 | 18.9 | 4.8 | 18.7 | ns |
| | | B | 6.1 | 33.9 | 5.2 | 23.7 | 5 | 19.9 | 5 | 17.6 | |
| $t_{rA}$, $t_{fA}$ | A-port rise and fall times | | 0.7 | 5.1 | 0.7 | 5 | 1 | 5 | 0.7 | 5 | ns |
| $t_{rB}$, $t_{fB}$ | B-port rise and fall times | | 1 | 7.3 | 0.7 | 5 | 0.7 | 3.9 | 0.6 | 3.8 | ns |
| $t_{SK(O)}$ | Channel-to-channel skew | | | 0.8 | | 0.7 | | 0.6 | | 0.6 | ns |
| Max data rate | | | 52 | | 60 | | 60 | | 60 | | Mbps |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.1 | 6.4 | 1 | 5.3 | 0.9 | 4.7 | ns |
| | B | A | 1 | 7 | 0.6 | 5.6 | 0.3 | 4.4 | |
| $t_{en}$ | OE | A | | 1 | | 1 | | 1 | µs |
| | | B | | 1 | | 1 | | 1 | |
| $t_{dis}$ | OE | A | 5 | 16.9 | 4.9 | 15 | 4.5 | 13.8 | ns |
| | | B | 4.8 | 21.8 | 4.5 | 17.9 | 4.4 | 15.2 | |
| $t_{rA}$, $t_{fA}$ | A-port rise and fall times | | 0.8 | 3.6 | 0.6 | 3.6 | 0.5 | 3.5 | ns |
| $t_{rB}$, $t_{fB}$ | B-port rise and fall times | | 0.6 | 4.9 | 0.7 | 3.9 | 0.6 | 3.2 | ns |
| $t_{SK(O)}$ | Channel-to-channel skew | | | 0.4 | | 0.3 | | 0.3 | ns |
| Max data rate | | | 70 | | 100 | | 100 | | Mbps |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 0.9 | 4.9 | 0.8 | 4 | ns |
| | B | A | 0.5 | 5.4 | 0.2 | 4 | |
| $t_{en}$ | OE | A | | 1 | | 1 | µs |
| | | B | | 1 | | 1 | |
| $t_{dis}$ | OE | A | 4.5 | 13.9 | 4.1 | 12.4 | ns |
| | | B | 4.1 | 17.3 | 4 | 14.4 | |
| $t_{rA}$, $t_{fA}$ | A-port rise and fall times | | 0.5 | 3 | 0.5 | 3 | ns |
| $t_{rB}$, $t_{fB}$ | B-port rise and fall times | | 0.7 | 3.9 | 0.6 | 3.2 | ns |
| $t_{SK(O)}$ | Channel-to-channel skew | | | 0.4 | | 0.3 | ns |
| Max data rate | | | 100 | | 100 | | Mbps |

## Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | 1.2 V | 1.5 V | 1.8 V | 2.5 V | 2.5 V | 3.3 V | |
| | | | $V_{CCB}$ | | | | | | | |
| | | | 5 V | 1.8 V | 1.8 V | 1.8 V | 2.5 V | 5 V | 3.3 V to 5 V | |
| | | | TYP | TYP | TYP | TYP | TYP | TYP | TYP | |
| $C_{pdA}$ | A-port input, B-port output | $C_L$ = 0, f = 10 MHz, $t_r = t_f$ = 1 ns, OE = $V_{CCA}$ (outputs enabled) | 9 | 8 | 7 | 7 | 7 | 7 | 8 | pF |
| | B-port input, A-port output | | 12 | 11 | 11 | 11 | 11 | 11 | 11 | |
| $C_{pdB}$ | A-port input, B-port output | | 35 | 26 | 27 | 27 | 27 | 27 | 28 | |
| | B-port input, A-port output | | 26 | 19 | 18 | 18 | 18 | 20 | 21 | |
| $C_{pdA}$ | A-port input, B-port output | $C_L$ = 0, f = 10 MHz, $t_r = t_f$ = 1 ns, OE = GND (outputs disabled) | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | pF |
| | B-port input, A-port output | | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | |
| $C_{pdB}$ | A-port input, B-port output | | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.03 | |
| | B-port input, A-port output | | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | 0.03 | |

## PRINCIPLES OF OPERATION

### Applications

The TXB0108 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

### Architecture

The TXB0108 architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0108 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at $V_{CCO}$ = 1.2 V to 1.8 V, 50Ω at $V_{CCO}$ = 1.8 V to 3.3 V and 40Ω at $V_{CCO}$ = 3.3 V to 5 V.

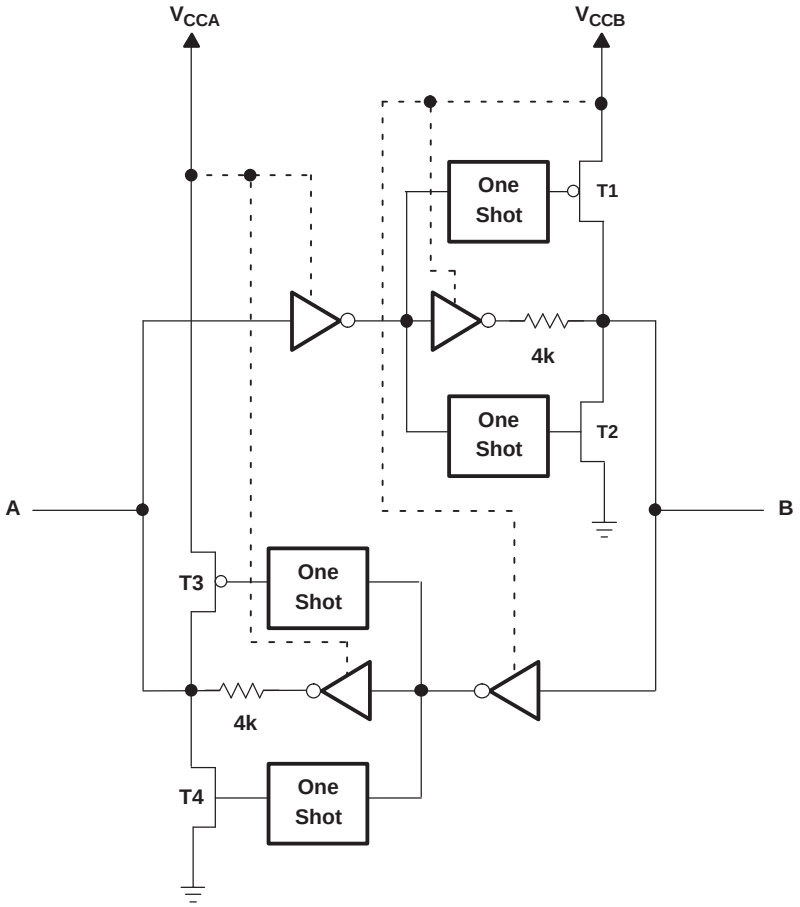
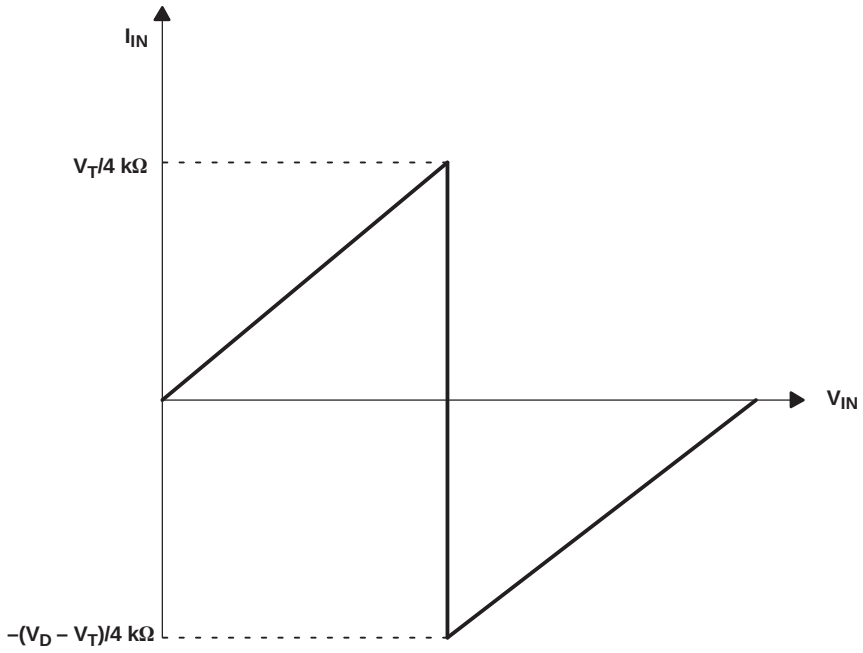



**Figure 1. Architecture of TXB0108 I/O Cell**

### Input Driver Requirements

Typical $I_{IN}$ vs $V_{IN}$ characteristics of the TXB0108 are shown in Figure 2. For proper operation, the device driving the data I/Os of the TXB0108 must have drive strength of at least ±2 mA.

## PRINCIPLES OF OPERATION (continued)




A. $V_T$ is the input threshold voltage of the TXB0108 (typically $V_{CCI}/2$).
B. $V_D$ is the supply voltage of the external driver.

**Figure 2. Typical $I_{IN}$ vs $V_{IN}$ Curve**

### Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0108 has circuitry that disables all output ports when either $V_{CC}$ is switched off ($V_{CCA/B}$ = 0 V).

### Enable and Disable

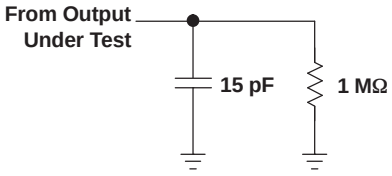
The TXB0108 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time ($t_{dis}$) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time ($t_{en}$) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

### Pullup or Pulldown Resistors on I/O Lines

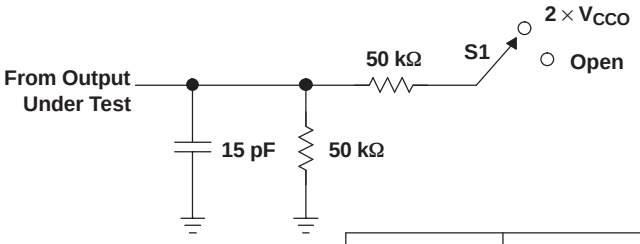
The TXB0108 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0108 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0108.

For the same reason, the TXB0108 should not be used in applications such as $I^2C$ or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

## PARAMETER MEASUREMENT INFORMATION

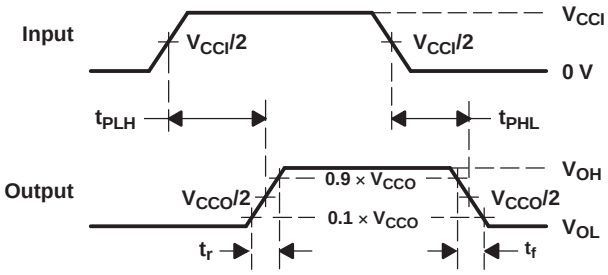



LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

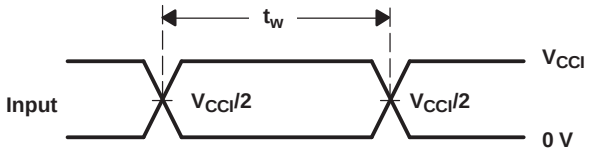



LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

| TEST | S1 |
|---|---|
| $t_{PZL}/t_{PLZ}$<br>$t_{PHZ}/t_{PZH}$ | $2 \times V_{CCO}$<br>Open |




VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS PULSE DURATION

A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
E. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
F. $V_{CCO}$ is the $V_{CC}$ associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TXB0108PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TXB0108PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TXB0108RGYR | ACTIVE | QFN | RGY | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TXB0108RGYRG4 | ACTIVE | QFN | RGY | 20 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TXB0108ZXYR | ACTIVE | BGA MICROSTAR JUNIOR | ZXY | 20 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

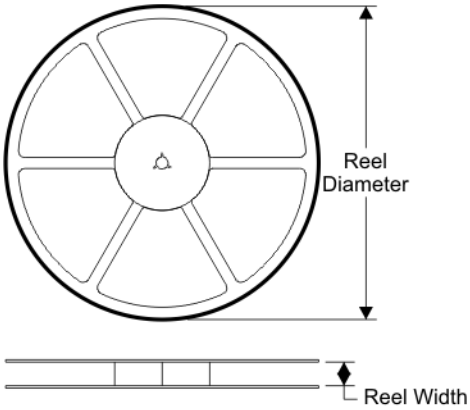
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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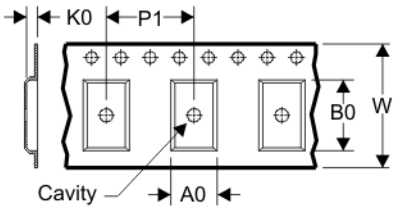
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## TAPE AND REEL BOX INFORMATION

**REEL DIMENSIONS**

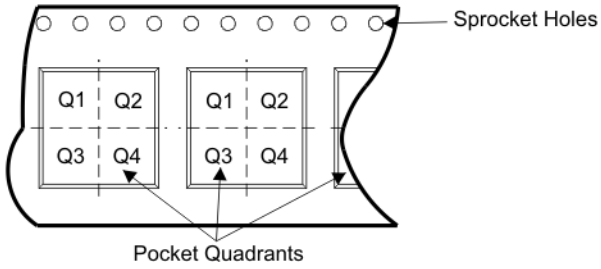



**TAPE DIMENSIONS**



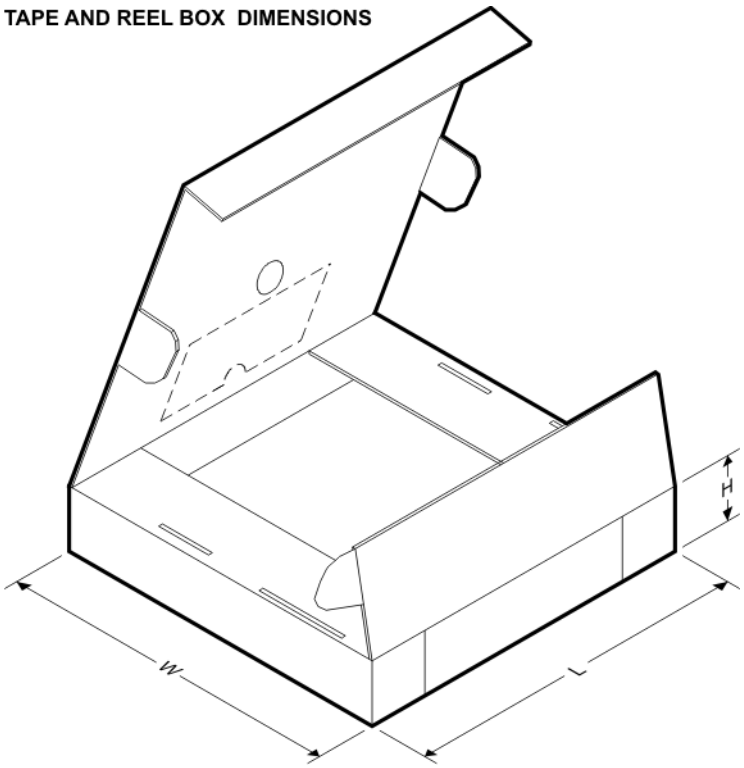

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



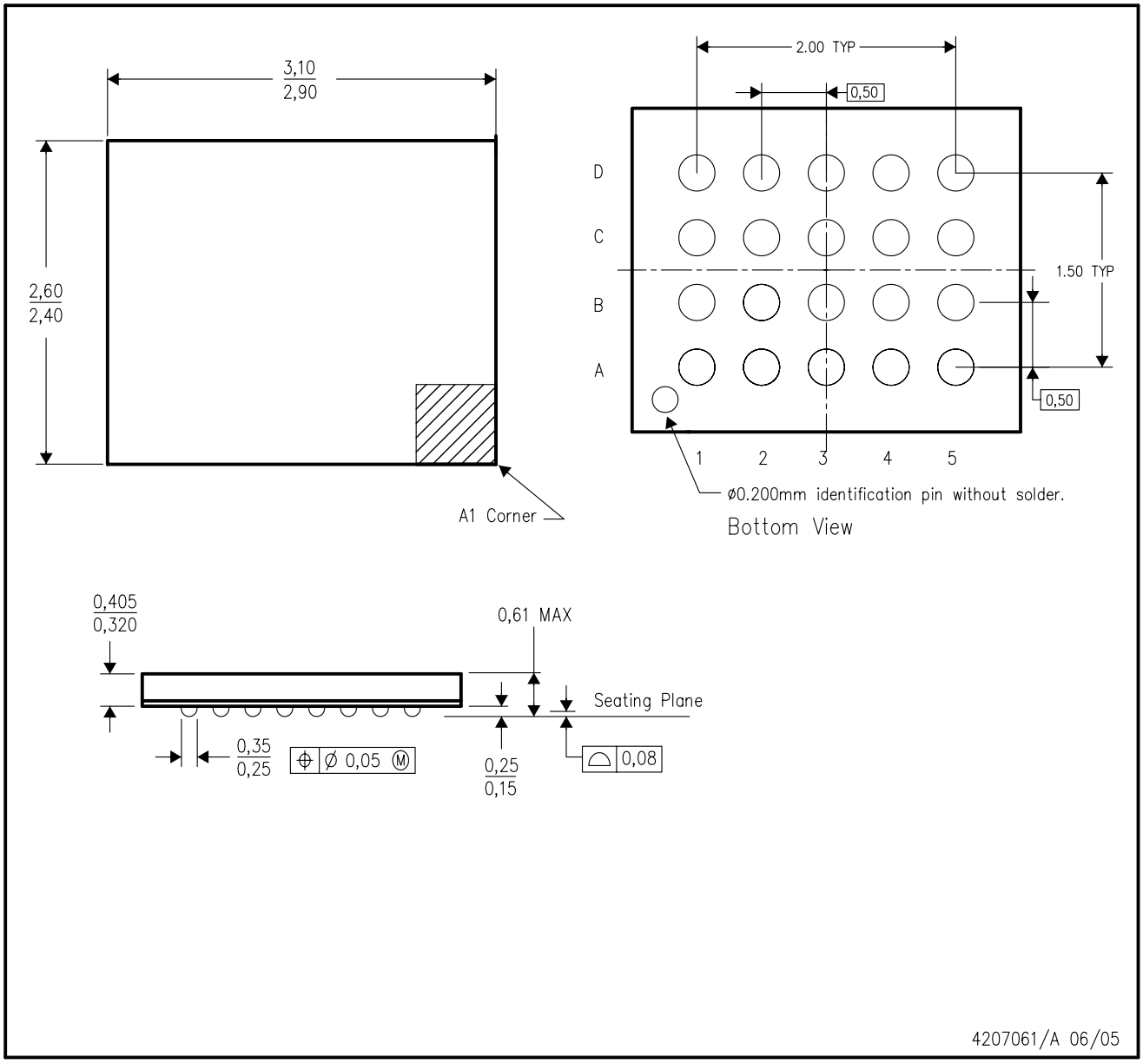

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TXB0108PWR | PW | 20 | SITE 41 | 330 | 16 | 7.0 | 7.0 | 2.0 | 8 | 16 | Q1 |
| TXB0108RGYR | RGY | 20 | SITE 41 | 180 | 12 | 4.0 | 5.0 | 2.0 | 8 | 12 | Q1 |
| TXB0108ZXYR | ZXY | 20 | SITE 60 | 330 | 12 | 3.0 | 3.0 | 1.0 | 4 | 12 | Q2 |

TAPE AND REEL BOX DIMENSIONS



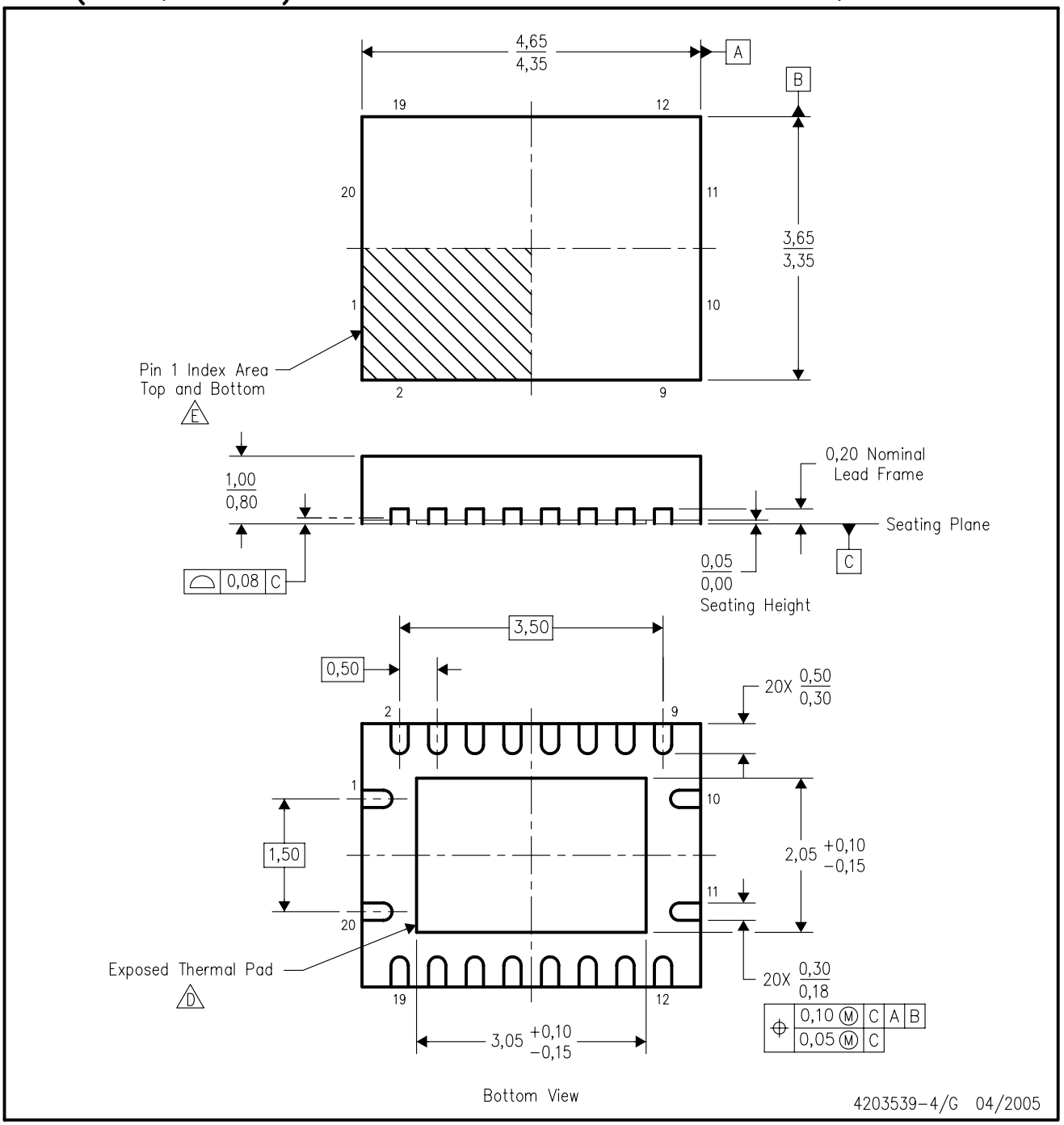

| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| TXB0108PWR | PW | 20 | SITE 41 | 346.0 | 346.0 | 33.0 |
| TXB0108RGYR | RGY | 20 | SITE 41 | 191.0 | 213.0 | 32.0 |
| TXB0108ZXYR | ZXY | 20 | SITE 60 | 343.0 | 338.0 | 21.0 |

ZXY (S–PBGA–N20) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is a lead–free solder ball design.

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BC.

# THERMAL PAD MECHANICAL DATA

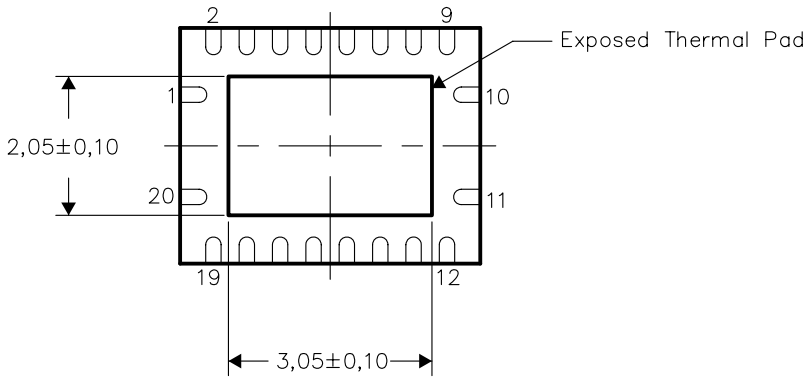
## RGY (R–PQFP–N20)

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

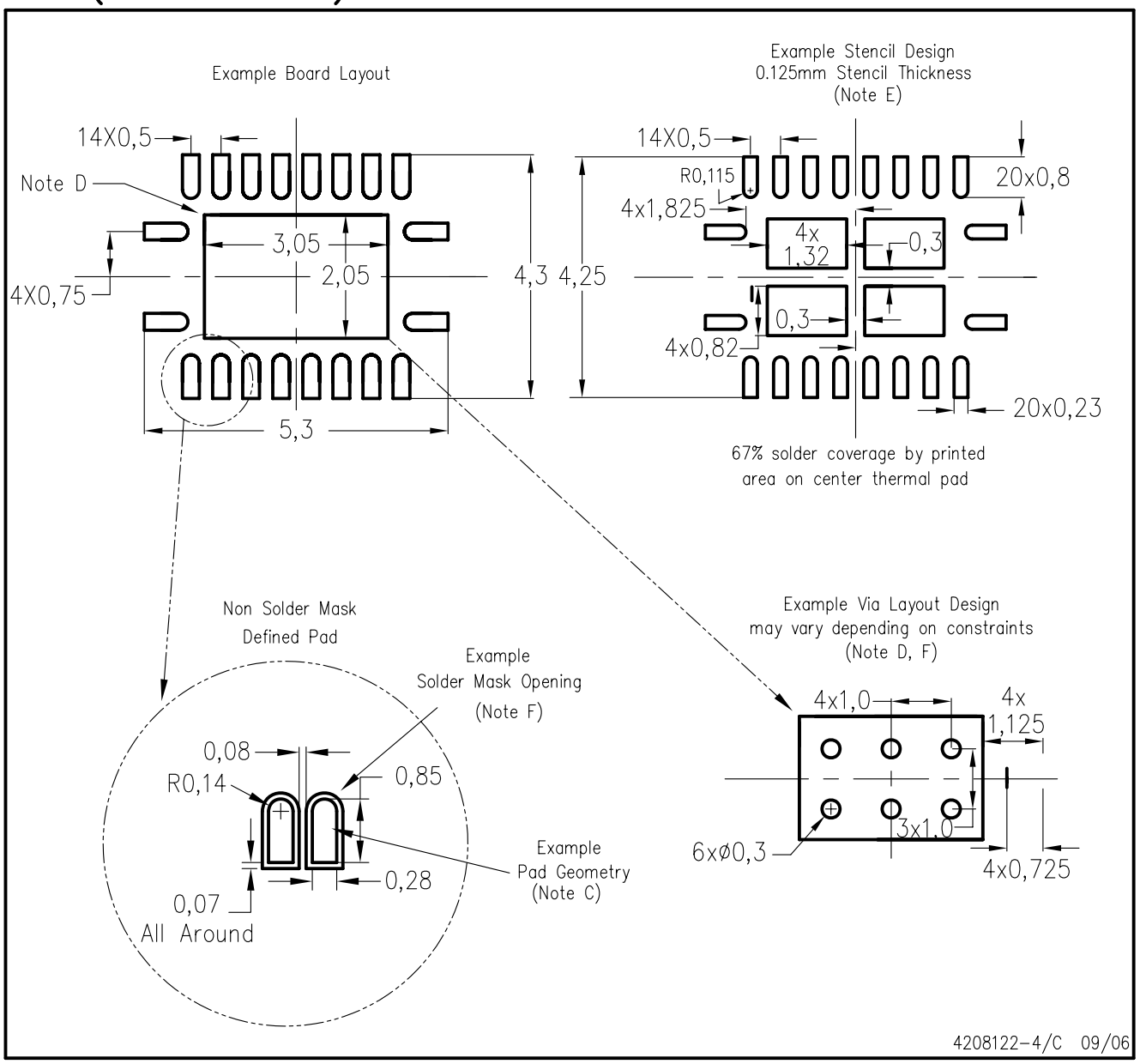



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

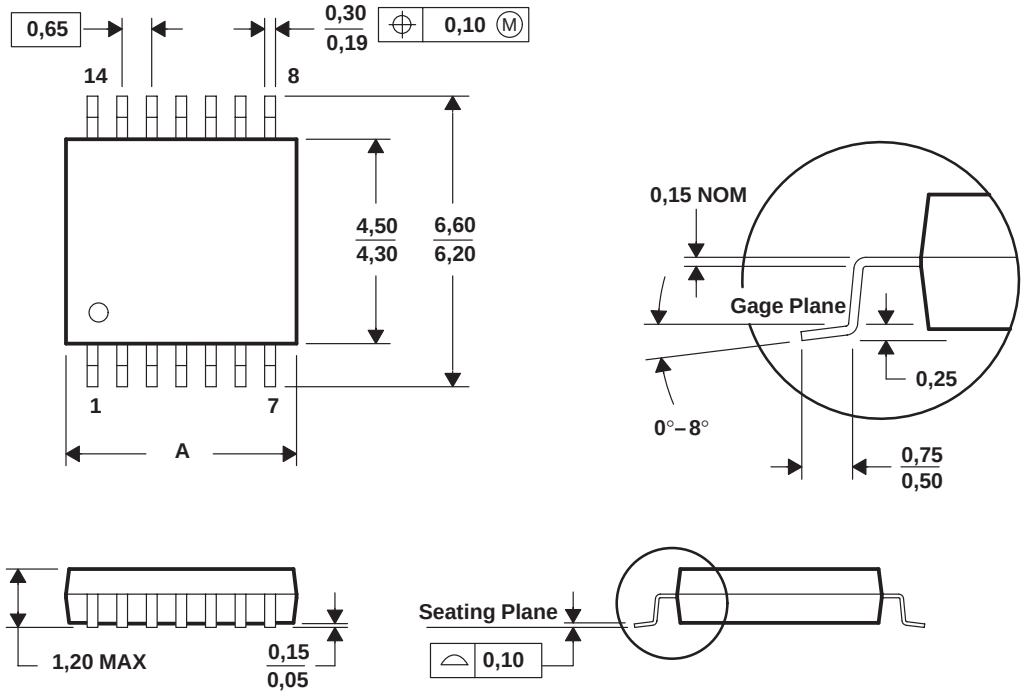
# RGY (R–PQFP–N20)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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