

2N7002BKV

60 V, 340 mA dual N-channel Trench MOSFET

Rev. 2 — 22 September 2010 Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

1.4 Quick reference data

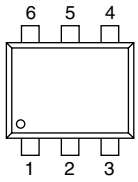
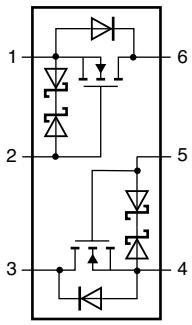
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_{amb} = 25 °C		-	-	60	V
V_{GS}	gate-source voltage	T_{amb} = 25 °C		-	-	±20	V
I_D	drain current	T_{amb} = 25 °C; V_{GS} = 10 V	[1]	-	-	340	mA
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 10 V; I_D = 500 mA		-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source 1		
2	G1	gate 1		
3	D2	drain 2		
4	S2	source 2		
5	G2	gate 2		
6	D1	drain 1		

017aaa055

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002BKV	-	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 4. Marking codes

Type number	Marking code
2N7002BKV	ZG

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_{amb} = 25 °C		-	60	V
V_{GS}	gate-source voltage	T_{amb} = 25 °C		-	±20	V
I_D	drain current	V_{GS} = 10 V	[1]			
		T_{amb} = 25 °C		-	340	mA
		T_{amb} = 100 °C		-	240	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \leq 10$ μs		-	1.2	A

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

Table 5. Limiting values *...continued*

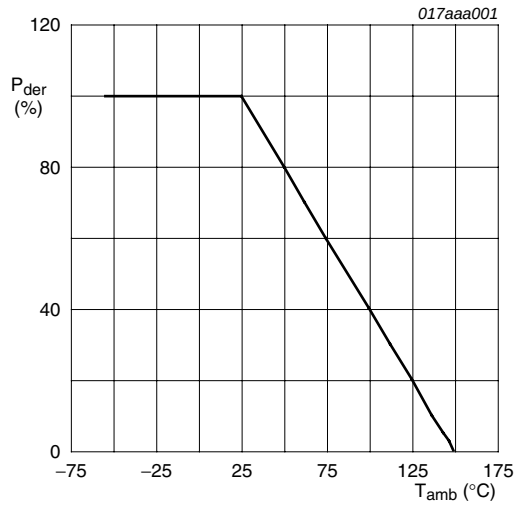
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	350	mW
			[1]	-	410	mW
		T_{sp} = 25 °C		-	1140	mW
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	340	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	human body model	[3]	-	2000	V
Per device						
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	525	mW
T_j	junction temperature				150	°C
T_{amb}	ambient temperature			−55	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

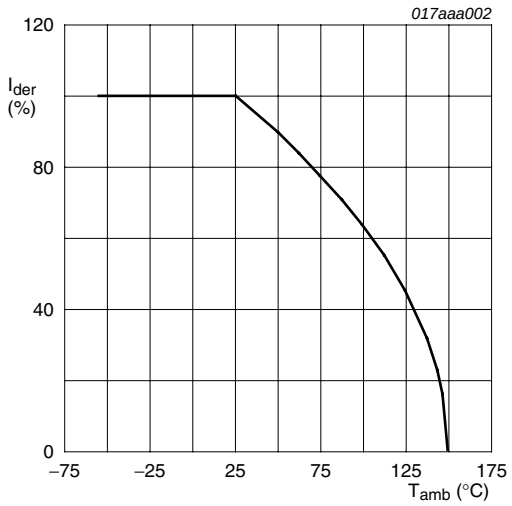
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature

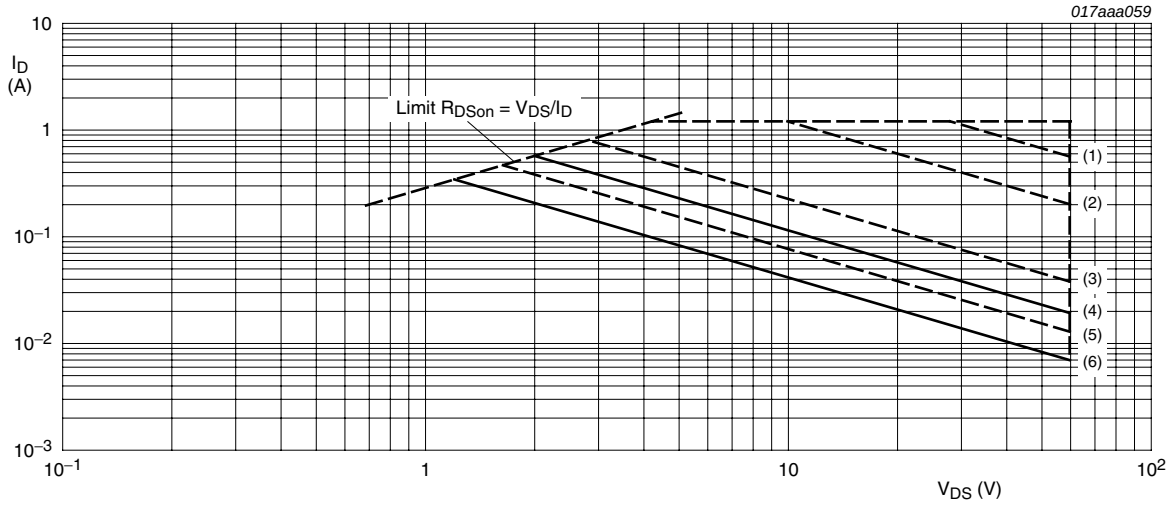


$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.



I_{DM} = single pulse

(1) t_p = 100 μs

(2) t_p = 1 ms

(3) t_p = 10 ms

(4) DC; T_{sp} = 25 °C

(5) t_p = 100 ms

(6) DC; T_{amb} = 25 °C; drain mounting pad 1 cm^2

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

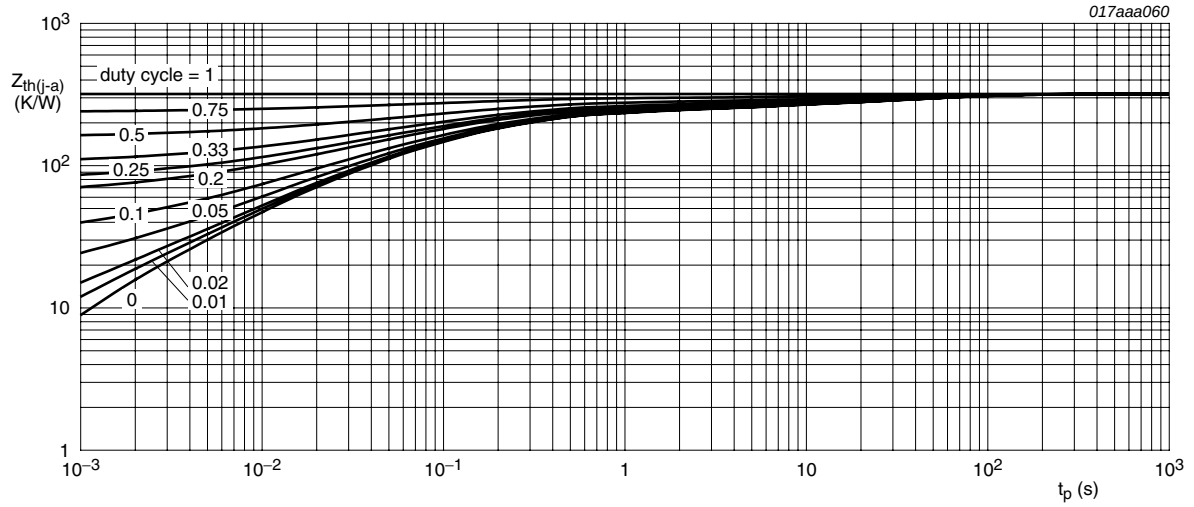
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	315	360	K/W
			[2]	-	265	305	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	110	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	240	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

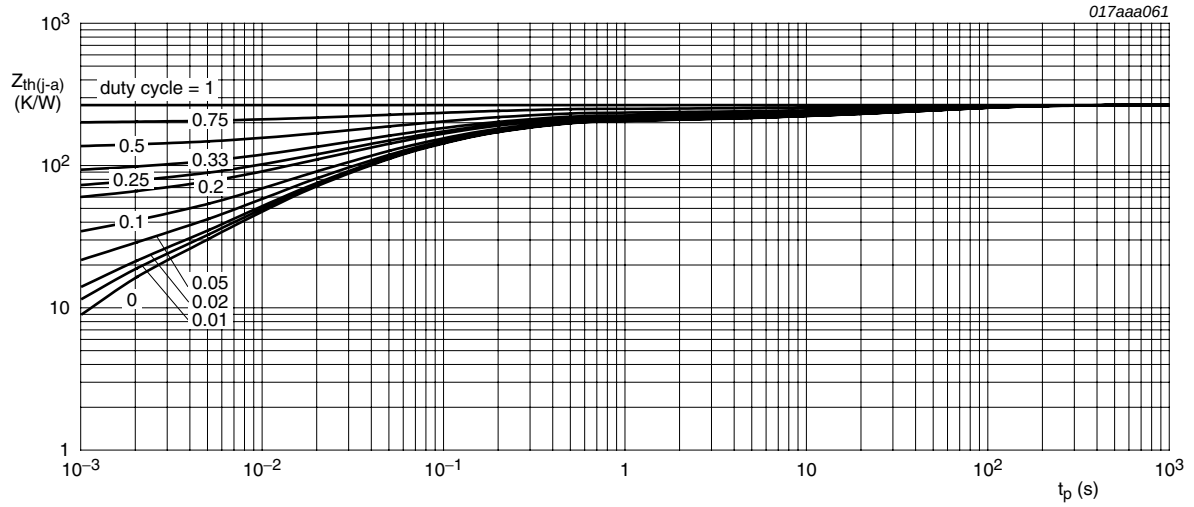
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm^2

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

7. Characteristics

Table 7. Characteristics

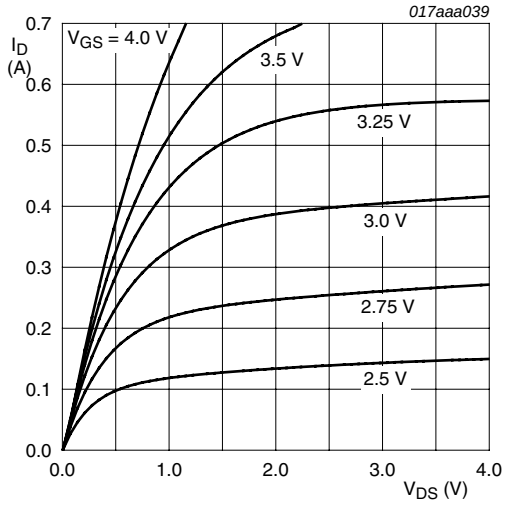
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0 V		60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 250 μA; V_{DS} = V_{GS}		1.1	1.6	2.1	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V					
		T_j = 25 °C		-	-	1	μA
		T_j = 150 °C		-	-	10	μA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V		-	-	10	μA
R_{DSon}	drain-source on-state resistance		[1]				
		V_{GS} = 5 V; I_D = 50 mA		-	1.3	2	Ω
		V_{GS} = 10 V; I_D = 500 mA		-	1	1.6	Ω
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 200 mA	[1]	-	550	-	mS
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 300 mA; V_{DS} = 30 V; V_{GS} = 4.5 V		-	0.5	0.6	nC
Q_{GS}	gate-source charge			-	0.2	-	nC
Q_{GD}	gate-drain charge			-	0.1	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 10 V; f = 1 MHz		-	33	50	pF
C_{oss}	output capacitance			-	7	-	pF
C_{rss}	reverse transfer capacitance			-	4	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 50 V; R_L = 250 Ω; V_{GS} = 10 V; R_G = 6 Ω		-	5	10	ns
t_r	rise time			-	6	-	ns
$t_{d(off)}$	turn-off delay time			-	12	24	ns
t_f	fall time			-	7	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 115 mA; V_{GS} = 0 V		0.47	0.75	1.1	V

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.01$.

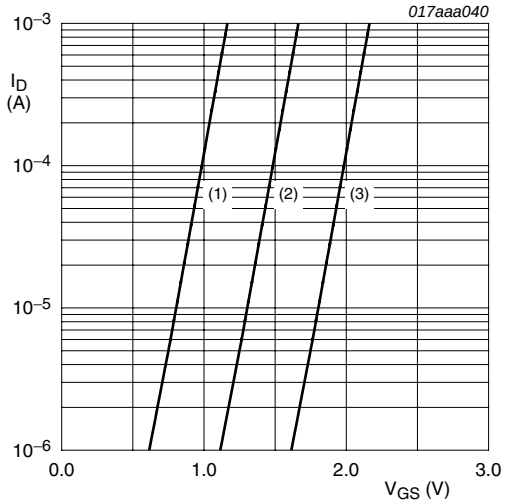
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.



T_{amb} = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



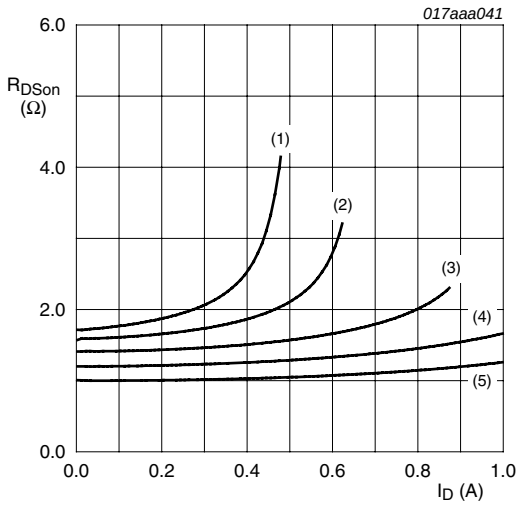
T_{amb} = 25 °C; V_{DS} = 5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage



T_{amb} = 25 °C

(1) V_{GS} = 3.25 V

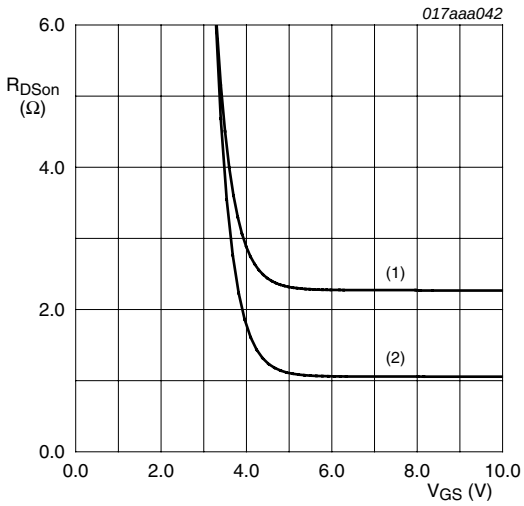
(2) V_{GS} = 3.5 V

(3) V_{GS} = 4 V

(4) V_{GS} = 5 V

(5) V_{GS} = 10 V

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



I_D = 500 mA

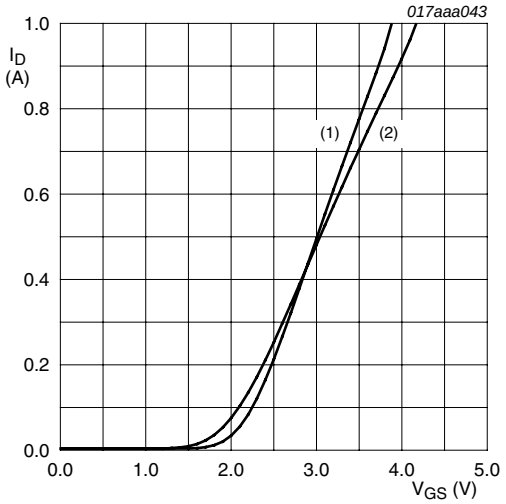
(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

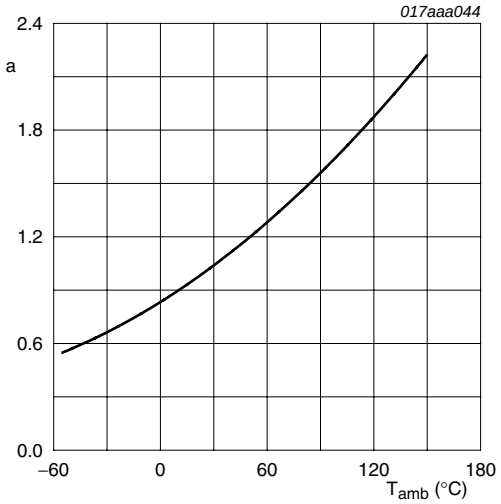


$V_{DS} > I_D \times R_{DSon}$

(1) T_{amb} = 25 °C

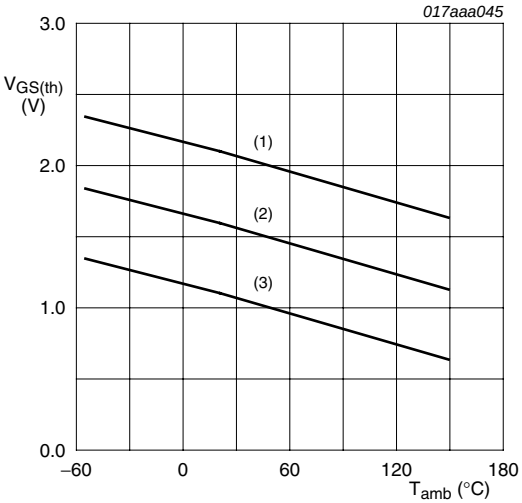
(2) T_{amb} = 150 °C

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values



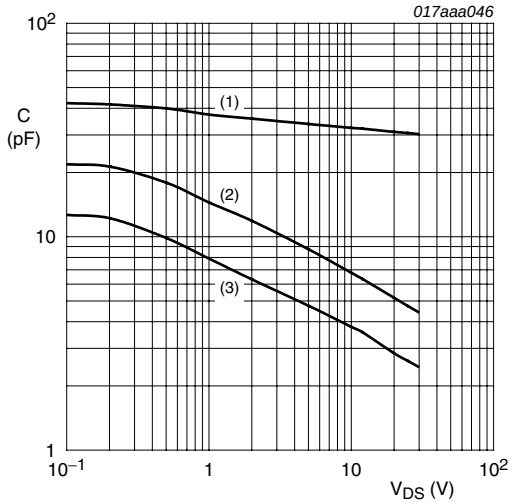
I_D = 0.25 mA; $V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of ambient temperature



f = 1 MHz; V_{GS} = 0 V

(1) C_{iss}

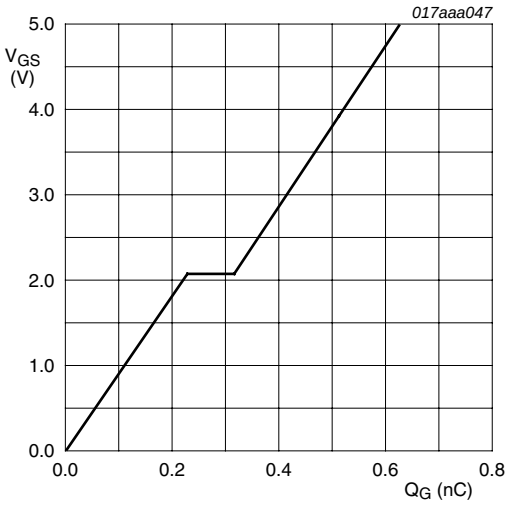
(2) C_{oss}

(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.



I_D = 300 mA; V_{DD} = 6 V; T_{amb} = 25 °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

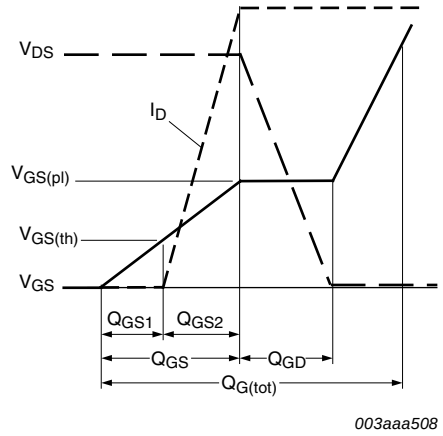
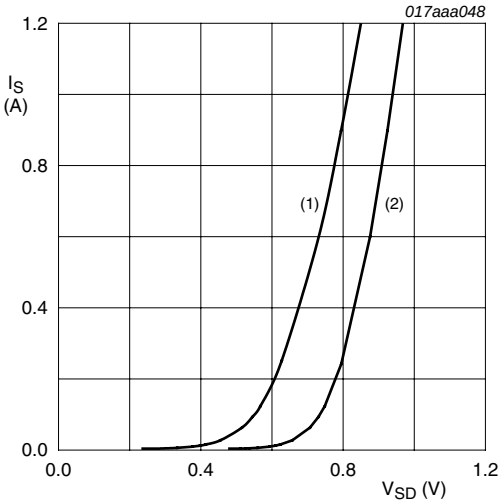


Fig 15. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

Fig 16. Source current as a function of source-drain voltage; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

8. Test information

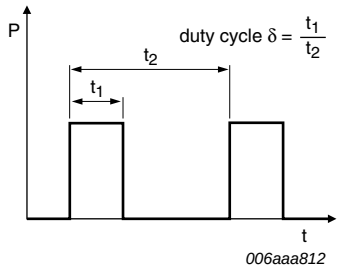


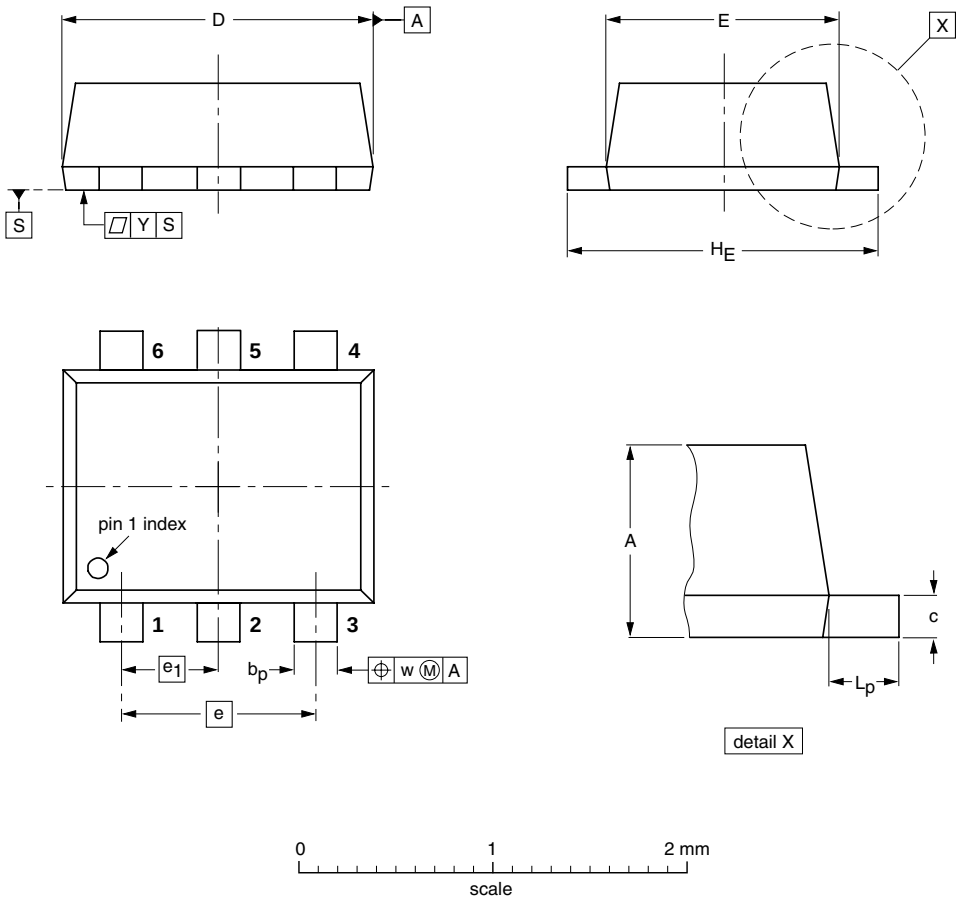
Fig 17. Duty cycle definition

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

9. Package outline

Plastic surface-mounted package; 6 leads **SOT666**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

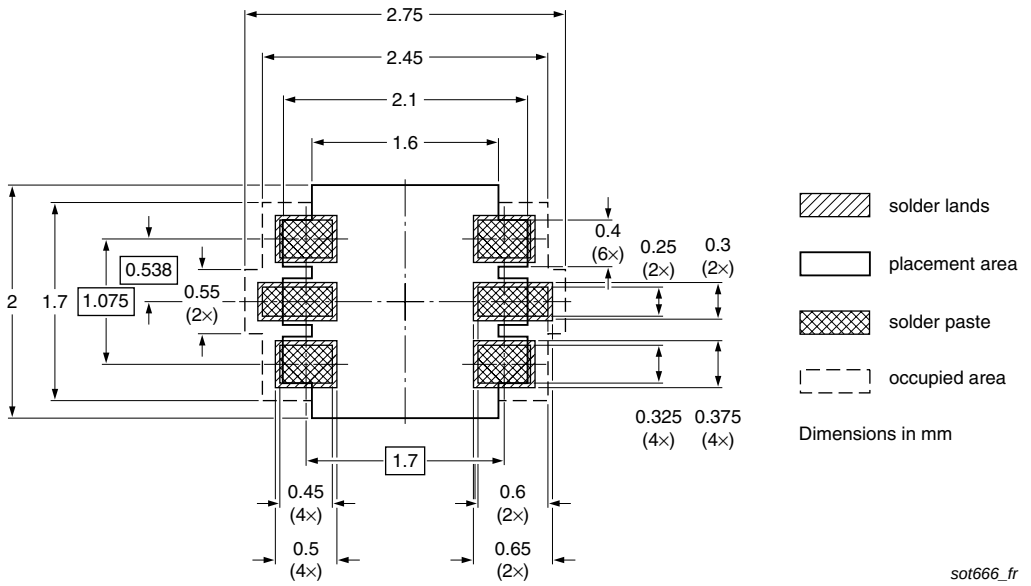
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						~~04-11-08~~ 06-03-16

Fig 18. Package outline SOT666

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

10. Soldering



Reflow soldering is the only recommended soldering method.

Fig 19. Reflow soldering footprint SOT666

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
2N7002BKV v.2	20100922	Product data sheet	-	2N7002BKV v.1
Modifications:	• Table 2 “Pinning”: graphic symbol amended • Table 6 “Thermal characteristics”: typo for $R_{th(j-sp)}$ maximum value per transistor amended • Table 6 “Thermal characteristics”: typo for $R_{th(j-a)}$ maximum value per device amended			
2N7002BKV v.1	20100610	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.