# 300mA, Ultra-Low Noise, Ultra-Fast CMOS LDO Regulator

## General Description

The RT9193 is designed for portable RF and wireless applications with demanding performance and space requirements. The RT9193 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The RT9193 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The RT9193 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the SC-70-5, SOT-23-5, TSOT-23-5, WDFN-6L 2x2 and MSOP-8 packages.

## Ordering Information

RT9193-□□□□

Package Type
U5 : SC-70-5
B : SOT-23-5
J5 : TSOT-23-5
QW : WDFN-6L 2x2 (W-Type)
F : MSOP-8

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Output Voltage
15 : 1.5V
16 : 1.6V
:
49 : 4.9V
50 : 5.0V
1H : 1.85V
2H : 2.85V
4G : 4.75V
(1.5V to 5V with 0.1V step is available)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Features

- **Ultra Low Noise for RF Application**
- **Ultra Fast Response in Line/Load Transient**
- **Quick Start-Up (Typically 50μs)**
- **<0.01μA Standby Current When Shutdown**
- **Low Dropout : 220mV @ 300mA**
- **Wide Operating Voltage Ranges : 2.5V to 5.5V**
- **TTL-Logic-Controlled Shutdown Input**
- **Low Temperature Coefficient**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **Only 1μF Output Capacitor Required for Stability**
- **High Power Supply Rejection Ratio**
- **Custom Voltage Available**
- **RoHS Compliant and 100% Lead (Pb)-Free**

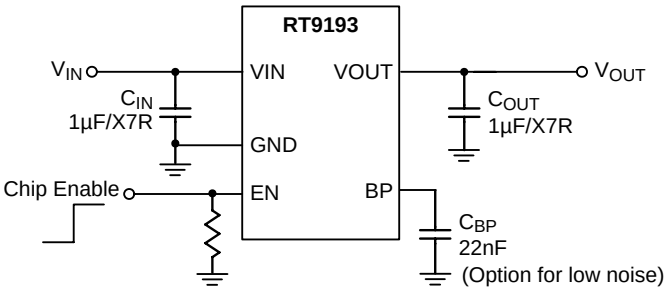
## Applications

- CDMA/GSM Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

## Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

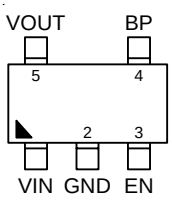
## Typical Application Circuit



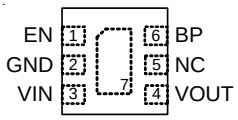

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## Pin Configurations

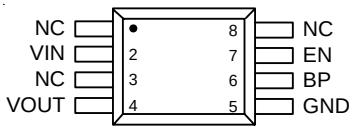
(TOP VIEW)




SC-70-5/SOT-23-5/TSOT-23-5




WDFN-6L 2x2

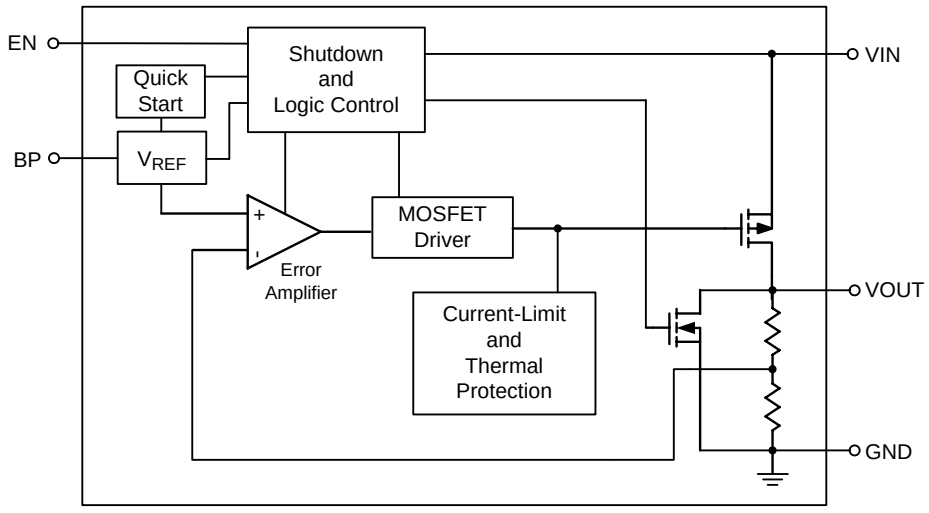



MSOP-8

## Functional Pin Description

| Pin Name | Pin Function |
|---|---|
| EN | Chip Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating. |
| BP | Reference Noise Bypass. This pin can be floating. For lowest noise performance, connect a 22nF capacitor between the BP and GND pins. |
| GND | Ground. |
| VOUT | Output Voltage. |
| VIN | Power Input Voltage. |

## Function Block Diagram




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## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  - SC-70-5 ---------- 300mW
  - TSOT-23-5/SOT-23-5 ---------- 400mW
  - WDFN-6L 2x2 ---------- 606mW
  - MSOP-8 ---------- 625mW
- Package Thermal Resistance (Note 2)
  - SOT-70-5, $\theta_{JA}$ ---------- 333°C/W
  - TSOT-23-5/SOT-23-5, $\theta_{JA}$ ---------- 250°C/W
  - TSOT-23-5/SOT-23-5, $\theta_{JC}$ ---------- 25°C/W
  - WDFN-6L 2x2, $\theta_{JA}$ ---------- 165°C/W
  - WDFN-6L 2x2, $\theta_{JC}$ ---------- 20°C/W
  - MSOP-8 $\theta_{JA}$ ---------- 160°C/W
  - MSOP-8 $\theta_{JC}$ ---------- 55°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.5V to 5.5V
- EN Input Voltage ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = $V_{OUT}$ + 1V, $C_{IN}$ = $C_{OUT}$ = 1µF, $C_{BP}$ = 22nF, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage Accuracy | $\Delta V_{OUT}$ | $I_{OUT}$ = 1mA | –2 | -- | 2 | % |
| Current Limit | $I_{LIM}$ | $R_{LOAD}$ = 1Ω | 360 | 400 | -- | mA |
| Quiescent Current | $I_Q$ | $V_{EN} \geq$ 1.2V, $I_{OUT}$ = 0mA | -- | 90 | 130 | µA |
| Dropout Voltage (Note 5) | $V_{DROP}$ | $I_{OUT}$ = 200mA, $V_{OUT}$ > 2.8V | | 170 | 200 | mV |
| | | $I_{OUT}$ = 300mA, $V_{OUT}$ > 2.8V | -- | 220 | 300 | |
| Line Regulation | $\Delta V_{LINE}$ | $V_{IN}$ = ($V_{OUT}$ + 1V) to 5.5V, $I_{OUT}$ = 1mA | -- | -- | 0.3 | % |
| Load Regulation | $\Delta V_{LOAD}$ | 1mA < $I_{OUT}$ < 300mA | -- | -- | 0.6 | % |
| Standby Current | $I_{STBY}$ | $V_{EN}$ = GND, Shutdown | -- | 0.01 | 1 | µA |

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| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| EN Input Bias Current | | $I_{IBSD}$ | $V_{EN}$ = GND or VIN | -- | 0 | 100 | nA |
| EN Threshold Voltage | Logic-Low | $V_{IL}$ | $V_{IN}$ = 3V to 5.5V, Shutdown | -- | -- | 0.4 | V |
| | Logic-High | $V_{IH}$ | $V_{IN}$ = 3V to 5.5V, Start-Up | 1.2 | -- | -- | |
| Output Noise Voltage | | $e_{NO}$ | 10Hz to 100kHz, $I_{OUT}$ = 200mA $C_{OUT}$ = 1μF | -- | 100 | -- | $\mu V_{RMS}$ |
| Power Supply Rejection Rate | f = 100Hz | PSRR | $C_{OUT}$ = 1μF, $I_{OUT}$ = 10mA | -- | –70 | -- | dB |
| | f = 10kHz | | | -- | –50 | -- | |
| Thermal Shutdown Temperature | | $T_{SD}$ | | -- | 165 | -- | °C |
| Thermal Shutdown Temperature | | ΔTSD | | -- | 30 | -- | °C |

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

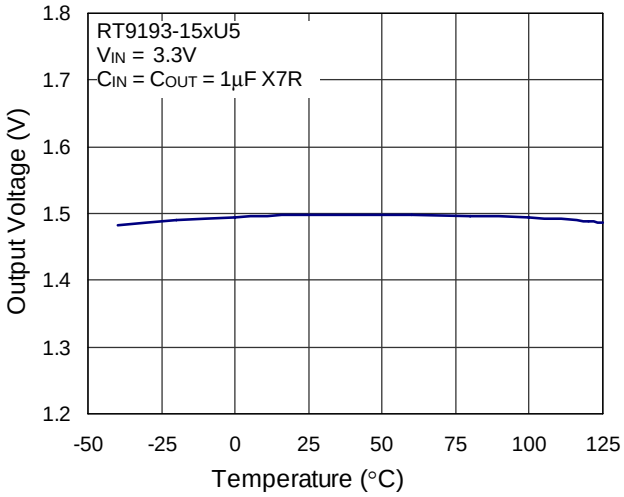
**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when $V_{OUT}$ is $V_{OUT(NORMAL)}$ – 100mV.

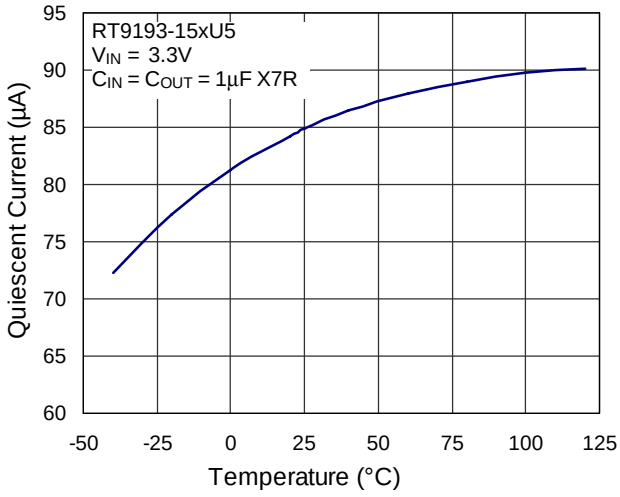
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## Typical Operating Characteristics

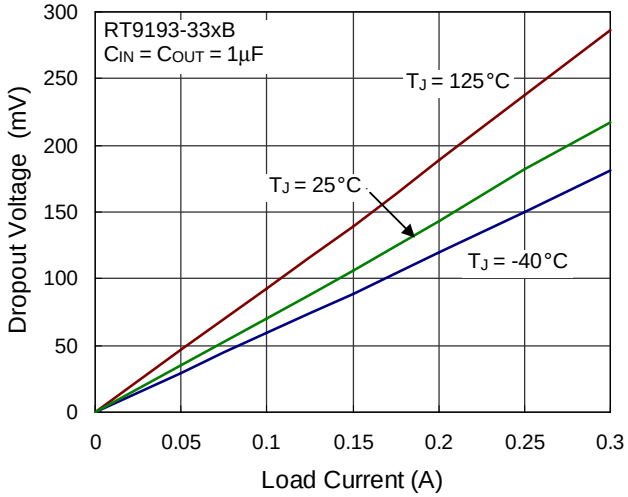
### Output Voltage vs. Temperature



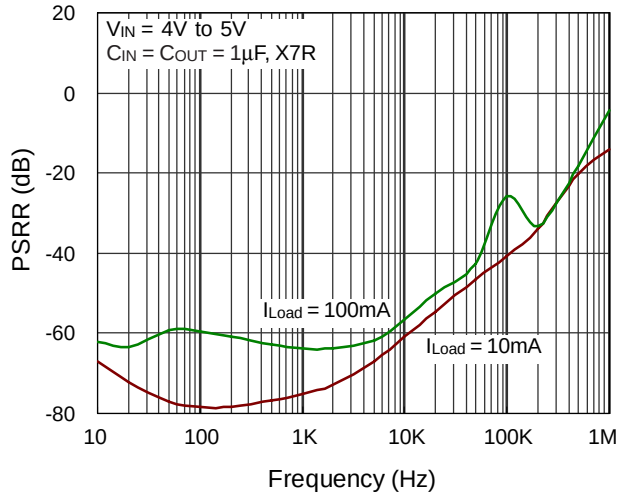

### Quiescent Current vs. Temperature



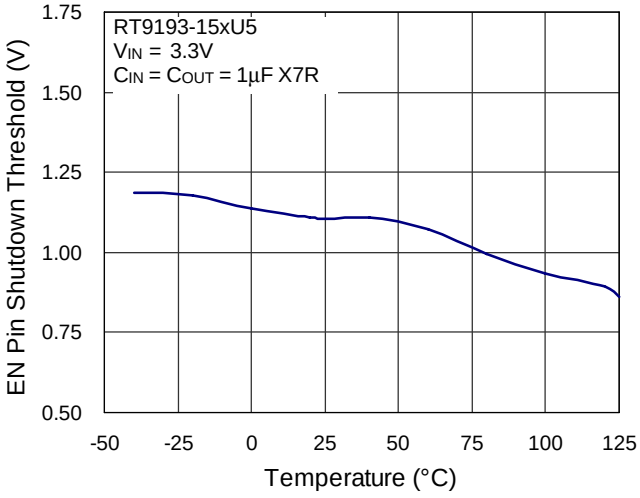

### Dropout Voltage vs. Load Current



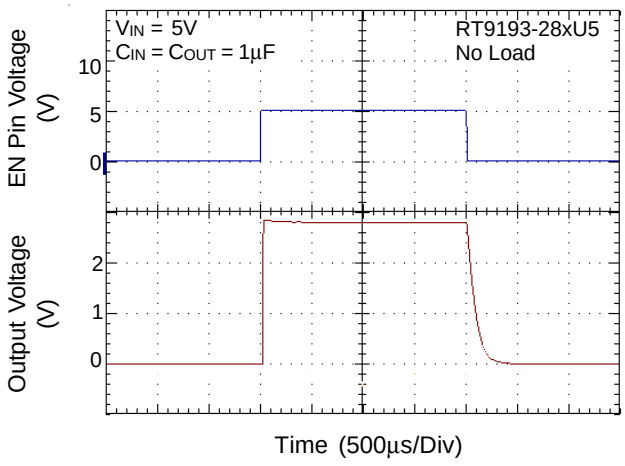

### PSRR




### EN Pin Shutdown Threshold vs. Temperature

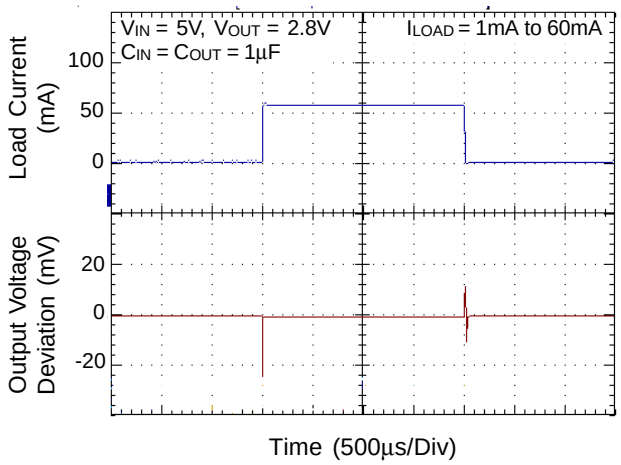



### EN Pin Shutdown Response

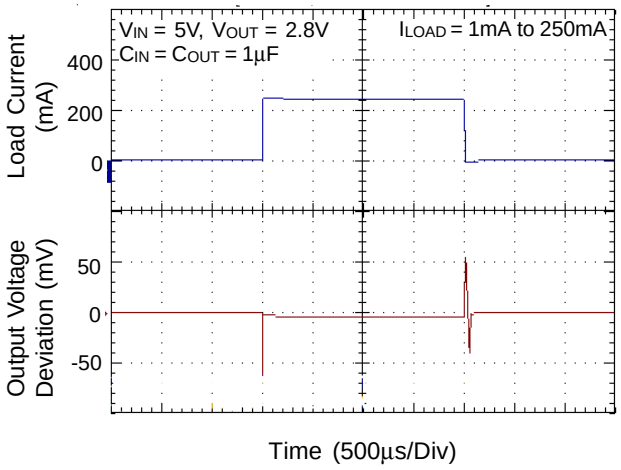



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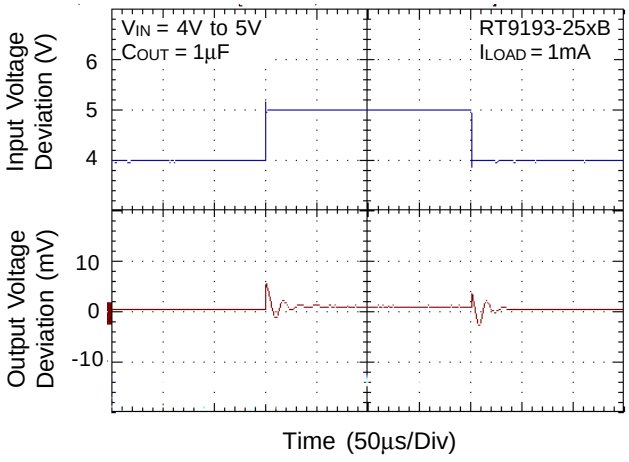
### Load Transient Response



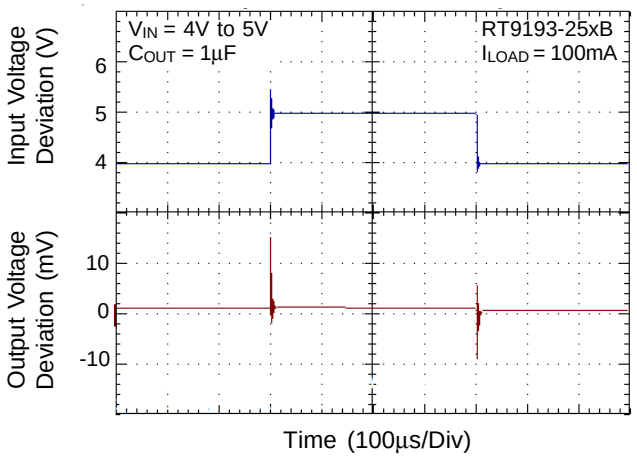

### Load Transient Response



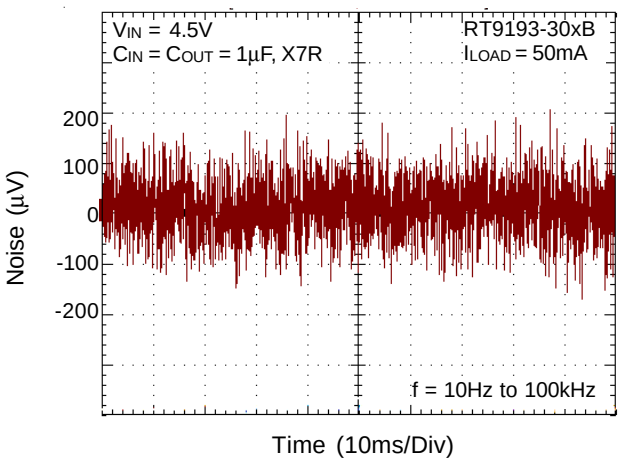

### Line Transient Response



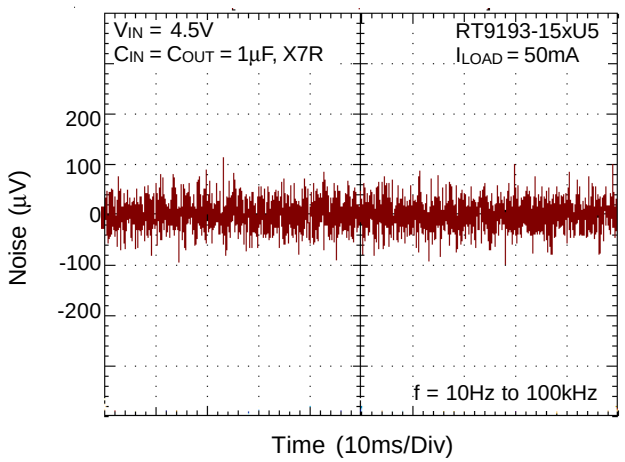

### Line Transient Response



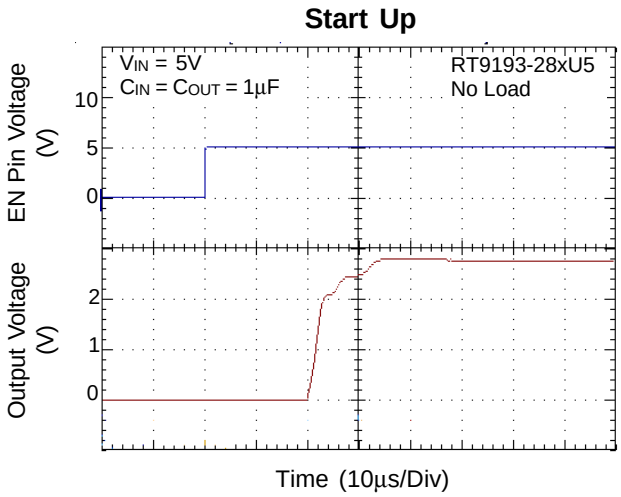

### Noise




### Noise




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## Applications Information

Like any low dropout regulator, the external capacitors used with the RT9193 must be carefully selected for regulator stability and performance. Using a capacitor whose value is >1μF on the RT9193 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9193 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is >1mΩ on the RT9193 output ensures stability. The RT9193 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the $V_{OUT}$ pin of the RT9193 and returned to a clean analog ground.

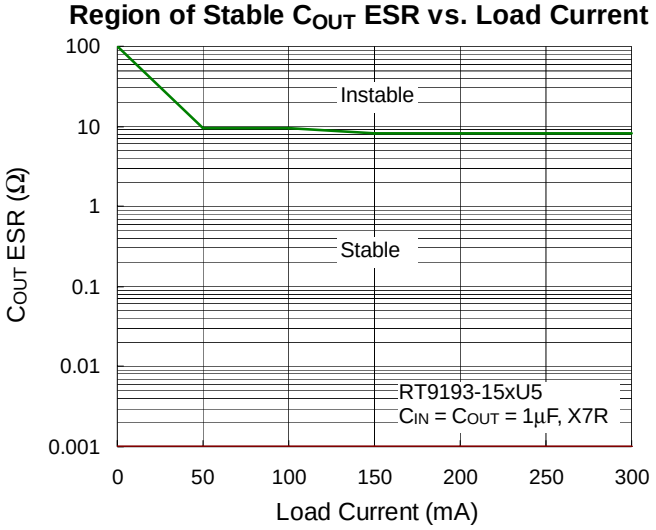



Figure 1

### Bypass Capacitor and Low Noise

Connecting a 22nF between the BP pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the BP pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the bypass capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

### Enable Function

The RT9193 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the RT9193 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to $V_{IN}$ to keep the LDO regulator in a continuously on state.

### Thermal Considerations

Thermal protection limits power dissipation in RT9193. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = ( T_{J(MAX)} - T_A ) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, $T_A$ is the ambient temperature and the $\theta_{JA}$ is the junction to ambient thermal resistance.

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For recommended operating conditions specification of RT9193, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and $T_A$ is the maximum ambient temperature. The junction to ambient thermal resistance ($\theta_{JA}$ is layout dependent) for TSOT-23-5/ SOT-23-5 package is 250°C/W, SC-70-5 package is 333°C/W, WDFN-6L 2x2 package is 165°C/W and MSOP-8 package is 160°C/W on standard JEDEC 51-3 thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 333 = 300mW for

SC-70-5

$P_{D(MAX)}$ = (125°C – 25°C) / 250 = 400mW for

TSOT-23-5/SOT-23-5

$P_{D(MAX)}$ = (125°C – 25°C) / 165 = 606mW for

WDFN-6L 2x2

$P_{D(MAX)}$ = (125°C –25°C) / 160 = 625mW for

MSOP-8

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance $\theta_{JA}$. For RT9193 packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

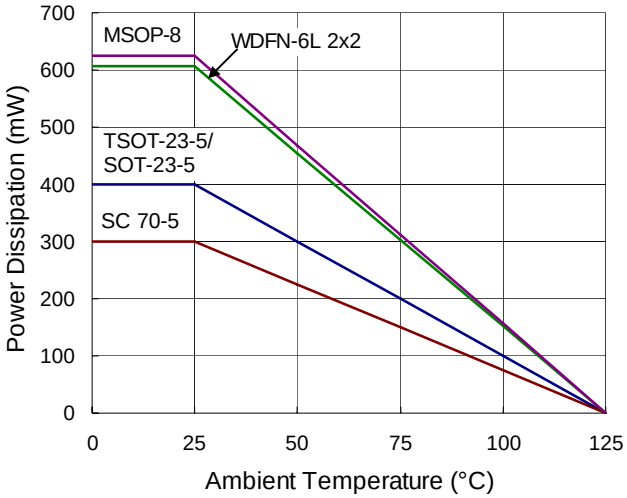
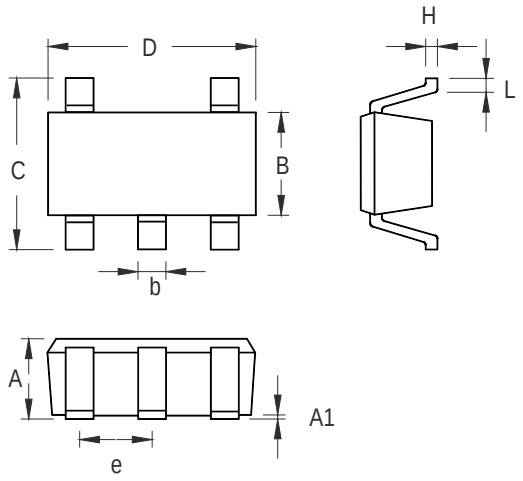



Figure 2. Derating Curve for Packages

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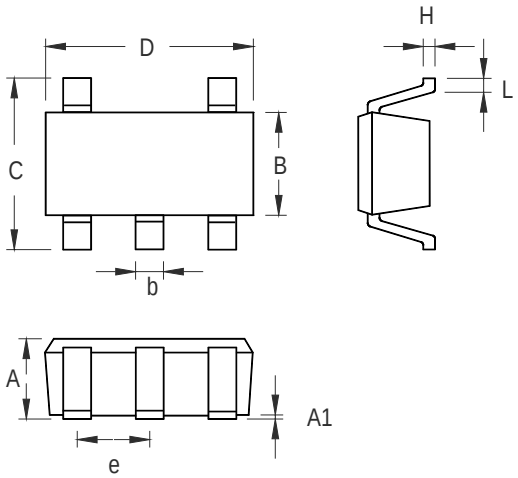
## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.800 | 1.100 | 0.031 | 0.044 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| B | 1.150 | 1.350 | 0.045 | 0.054 |
| b | 0.150 | 0.400 | 0.006 | 0.016 |
| C | 1.800 | 2.450 | 0.071 | 0.096 |
| D | 1.800 | 2.250 | 0.071 | 0.089 |
| e | 0.650 | | 0.026 | |
| H | 0.080 | 0.260 | 0.003 | 0.010 |
| L | 0.210 | 0.460 | 0.008 | 0.018 |

**SC-70-5 Surface Mount Package**

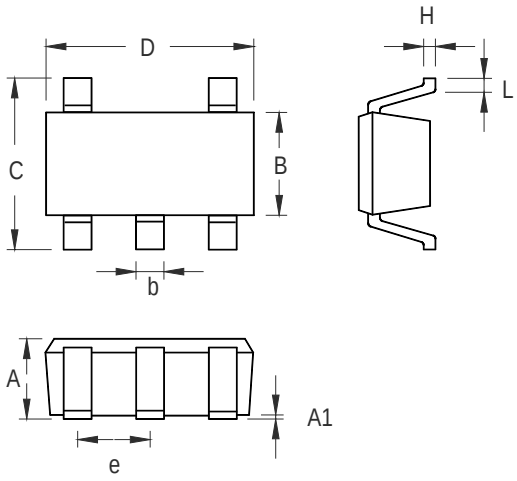
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| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 1.000 | 0.028 | 0.039 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.300 | 0.559 | 0.012 | 0.022 |
| C | 2.591 | 3.000 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**TSOT-23-5 Surface Mount Package**

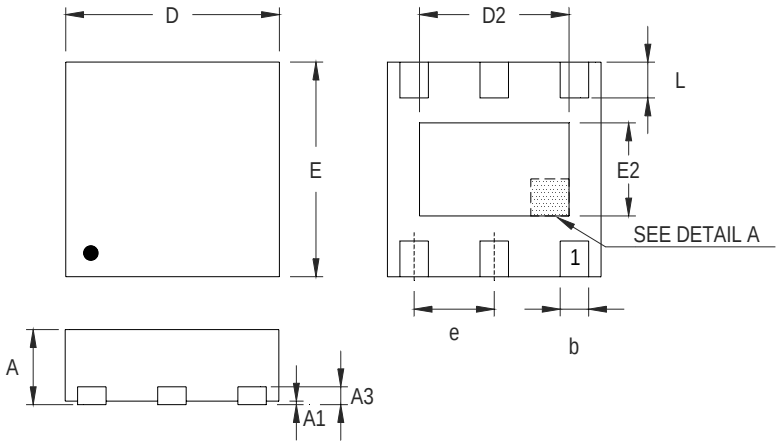
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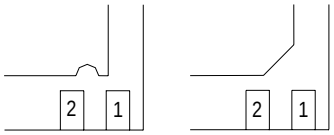



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.889 | 1.295 | 0.035 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.356 | 0.559 | 0.014 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**SOT-23-5 Surface Mount Package**

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**DETAIL A**

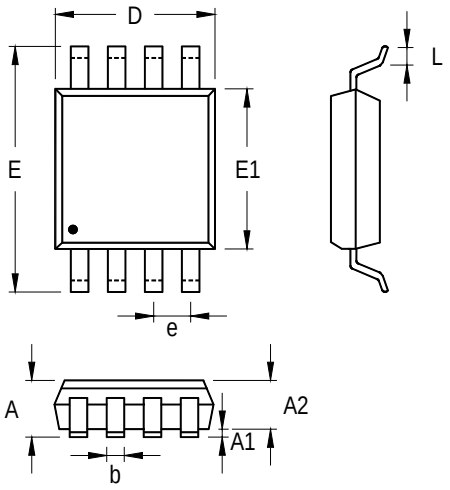
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.350 | 0.008 | 0.014 |
| D | 1.950 | 2.050 | 0.077 | 0.081 |
| D2 | 1.000 | 1.450 | 0.039 | 0.057 |
| E | 1.950 | 2.050 | 0.077 | 0.081 |
| E2 | 0.500 | 0.850 | 0.020 | 0.033 |
| e | 0.650 | | 0.026 | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

**W-Type 6L DFN 2x2 Package**

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| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.810 | 1.100 | 0.032 | 0.043 |
| A1 | 0.000 | 0.150 | 0.000 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.220 | 0.380 | 0.009 | 0.015 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| e | 0.650 | | 0.026 | |
| E | 4.800 | 5.000 | 0.189 | 0.197 |
| E1 | 2.900 | 3.100 | 0.114 | 0.122 |
| L | 0.400 | 0.800 | 0.016 | 0.031 |

**8-Lead MSOP Plastic Package**

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