**PAM8902H**

# 30 $V_{PP}$ MONO CLASS-D AUDIO AMPLIFIER FOR PIEZO/CERAMIC SPEAKERS

## Description

The PAM8902H is a mono, Class-D audio amplifier with integrated boost convertor designed for piezo and ceramic speakers.The PAM8902H is capable of driving a ceramic/ piezo speaker with 30Vpp(10.6Vrms) from a 3.6V power supply.The PAM8902H's Boost converter operates at a fixed frequency of 1.5MHz , and provides a 17.5V supply with a minimum number of external components. PAM8902H features an integrated audio low pass filter that rejects high frequency noise thus improving audio fidelity. And three gain modes of 21dB, 26dB and 32.5dB easy for using.PAM8902H also provides thermal ,short, under and over voltage protection.

The PAM8902H is available in a 16-ball 1.95mm x 1.95mm CSP package and 16-pin QFN4x4 package.

## Features

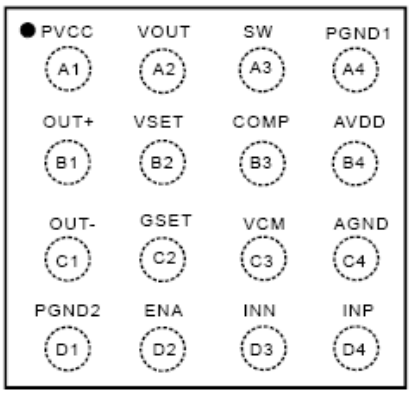
- Supply Voltage Range From 2.5V to 5.5V
- 30 $V_{PP}$ Output Load Voltage From a 2.5V Supply
- Integrated Boost Converter Generates 17.5V Supply
- Programmable Soft-Start
- Small Boost Converter Inductor
- Selectable Gain of 21dB, 26dB, and 32.5dB
- Selectable Boost Output Voltage of 8V, 12V, and 17.5V
- Low Shutdown Current: <1μA
- Build in Thermal , OCP ,OVP,Short Protection
- Available in Space Saving Packages:
  - 16-ball 1.95mmx1.95mm CSP Package
  - 16-pin QFN4x4 Package

## Applications

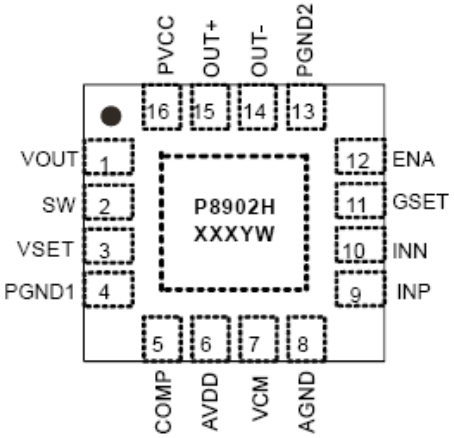
- Wireless or Cellular Handsets
- Portable DVD Player
- Personal Digital Assistants (PDAs )
- Electronic Dictionaries
- Digital Still Cameras

## Pin Assignments

16 Ball CSP
Top View



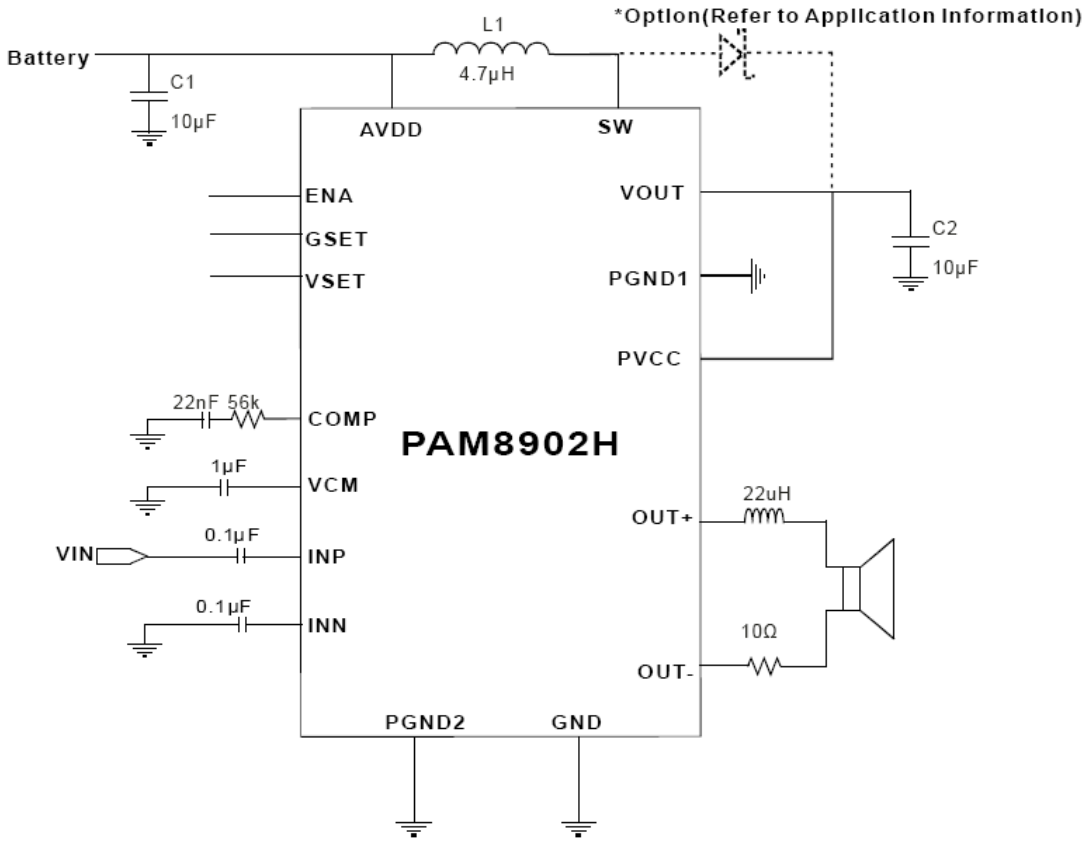

Top View
QFN 4X4 16L




● : Pin 1 Indicator


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## Typical Applications Circuit

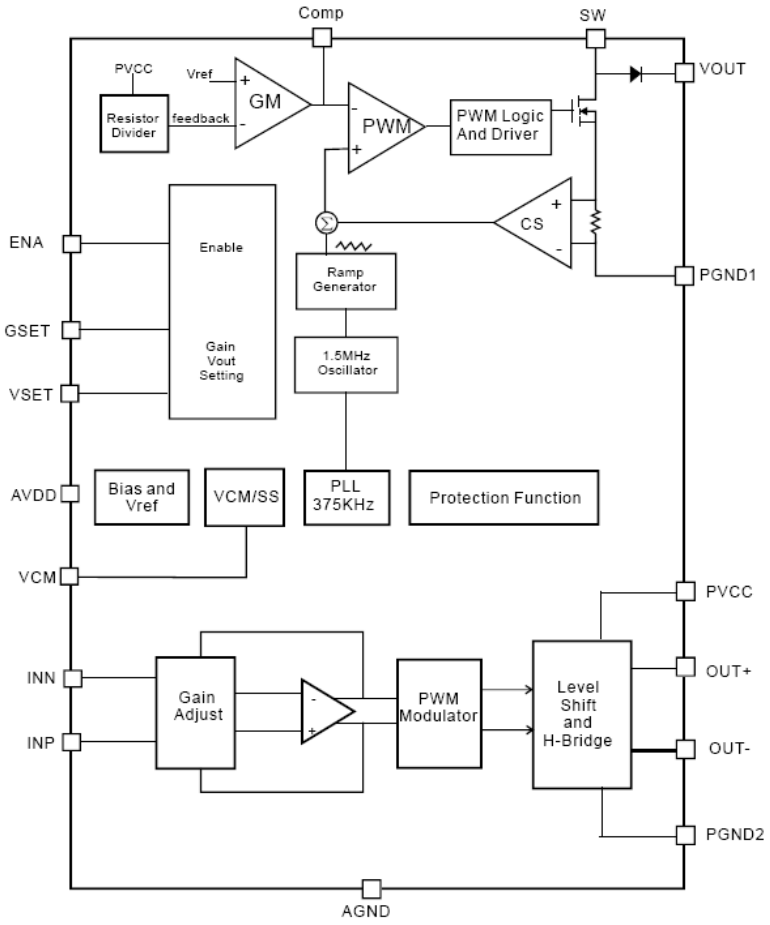



## Pin Descriptions

| Pin Name | Bump (CSP) | Pin Number (QFN) | Function |
|---|---|---|---|
| PVCC | A1 | 16 | Audio Amplifier Power Supply |
| VOUT | A2 | 1 | Boost Convertor Output |
| SW | A3 | 2 | Boost Convertor Switching Node |
| PGND1 | A4 | 4 | Boost Convertor Power Ground |
| OUT+ | B1 | 15 | Positive Differential Audio Output |
| VSET | B2 | 3 | Boost Convertor Output Voltage Setting (8V,12V,17.5V) |
| COMP | B3 | 5 | Boost Convertor compensation |
| AVDD | B4 | 6 | Power Supply |
| OUT- | C1 | 14 | Negative Differential Audio Output |
| GSET | C2 | 11 | Amplifier Gain setting ( 21dB , 26dB , 32.5dB) |
| VCM | C3 | 7 | Common Mode bypass Cap |
| AGND | C4 | 8 | Analog Ground |
| PGND2 | D1 | 13 | Class D Power Ground |
| ENA | D2 | 12 | Whole chip Enable |
| INN | D3 | 10 | Negative Differential Audio Input |
| INP | D4 | 9 | Positive Differential Audio Input |


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## Functional Block Diagram




## Absolute Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage | 6.0 | V |
| Input Voltage | -0.3 to $V_{DD}$ +0.3 | |
| Storage Temperature | -65 to 150 | °C |
| Maximum Junction Temperature | 150 | |
| Soldering Temperature | 250, 10sec | |

## Recommended Operating Conditions (@$T_A$ = +25°C, unless otherwise specified.)

| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage Range | 2.5 to 5.5 | V |
| Ambiient Temperature Range | -40 to +85 | °C |
| Junction Temperature Range | -40 to +125 | |


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## Thermal Information

| Parameter | Symbol | Package | Maximum | Unit |
|---|---|---|---|---|
| Thermal Resistance (Junction to Ambient) | $\theta_{JA}$ | CSP | 90 | °C/W |
| | | QFN4x4-16 | 52 | |
| Thermal Resistance (Junction to Case) | $\theta_{JC}$ | CSP | 72 | °C/W |
| | | QFN4x4-16 | 30 | |

## Electrical Characteristics (@$T_A$ = +25°C, $V_{DD}$ = 3.6V, $C_L$ = 1µF, $V_{SET}$ Float, unless otherwise specified.)

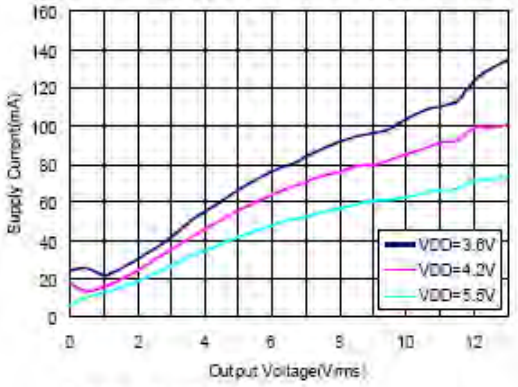
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Input Voltage | | 2.5 | | 5.5 | V |
| $I_Q$ | Quiescent Current | EN > 1.2V, VSET = High | | 30 | 48 | mA |
| | | EN > 1.2V, VSET = Floating | | 10 | 18 | |
| | | EN > 1.2V, VSET = GND | | 5 | 12 | |
| $I_{SD}$ | Shutdown Current | EN = 0V | | 0.1 | 1.0 | µA |
| $T_{WU}$ | Wake-Up Time | EN From Low to High | | 40 | | mS |
| $V_{EH}$ | Chip Enable | | 1.2 | | | V |
| $V_{EL}$ | Chip Disable | | | | 0.4 | |
| $V_H$ | GSET/VSET High | | $V_{DD}$ -0.5 | | $V_{DD}$ | V |
| $V_F$ | GSET/VSET Floating | | 1 | | $V_{DD}$ -1 | |
| $V_L$ | GSET/VSET Low | | 0 | | 0.5 | |
| UVLO | Under Voltage Lockout Threshold | $V_{DD}$ From High to Low | | 2.2 | | V |
| $UVLO_H$ | Under Voltage Lockout Hysteresis | $V_{DD}$ From Low to High | | 0.2 | | |
| OTP | Thermal Shutdown Threshold | | | 150 | | °C |
| $OTP_H$ | Thermal Shutdown Lockout Hysteresis | | | 30 | | °C |
| | | | | | | |
| **Boost Converter** | | | | | | |
| $V_O1$ | Output Voltage | VSET = GND, No Load | 7.2 | 8.0 | 8.8 | V |
| $V_O2$ | | VSET = NC, No Load | 10.8 | 12.0 | 13.2 | V |
| $V_O3$ | | VSET = AVDD, No Load | 16 | 17.5 | 19 | V |
| $C_L$ | Current Limit | Average Input Current | | 1.0 | | A |
| $R_{LS}$ | Low Side MOSFET $R_{DS(ON)}$ | $I_O$ = 50mA | | 0.5 | | Ω |
| $f_{OSCB}$ | Boost Switching Frequency | | 1.1 | 1.5 | 1.9 | MHz |
| | | | | | | |
| **Class-D** | | | | | | |
| $f_{OSCD}$ | Class-D Amplifier Switching Frequency | Input AC-GND | 225 | 375 | 475 | KHz |
| CMRR | Common Mode Reject Ratio | $V_{IN}$ = ±100mV, $V_{DD}$ = 3.6V | | 60 | | dB |
| $V_{OS}$ | Output Offset Voltage | Output Offset Voltage | | 5 | 50 | mV |
| $R_P$ | $R_{DS(ON)}$ | High Side | | 1.5 | | Ω |
| | | Low Side | | 0.6 | | Ω |
| $A_V1$ | Closed-Loop Voltage Gain | $G_{SET}$ = AVDD, $V_O$ = $1V_{RMS}$ | | 32.5 | | dB |
| $A_V2$ | | $G_{SET}$ = AVDD, $V_O$ = $1V_{RMS}$ | | 26 | | |
| $A_V3$ | | $G_{SET}$ = AVDD, $V_O$ = $1V_{RMS}$ | | 21 | | |
| PSRR | Power Supply Reject Ratio | 200m $V_{PP}$ Supply Ripple @ 217Hz | | 70 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | $V_O$ = $5V_{RMS}$ | | 0.3 | | % |
| SNR | Signal to Noise Ratio | Input AC Ground, A-Weighting | | 90 | | dB |


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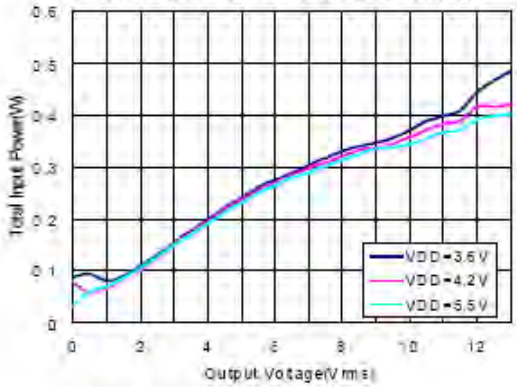
## Typical Operating Characteristics

(@$T_A$ = +25°C, $V_{DD}$ = 4.2V, Gain = 26dB, $C_{IN}$ = 1µF, $C_{LOAD}$ = 1µF, unless otherwise specified.)

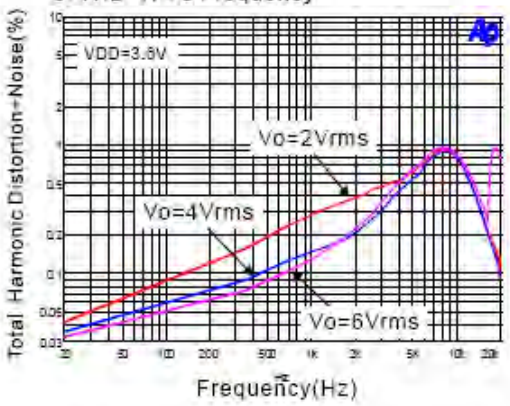
1. Total Supply Current VS Output Voltage



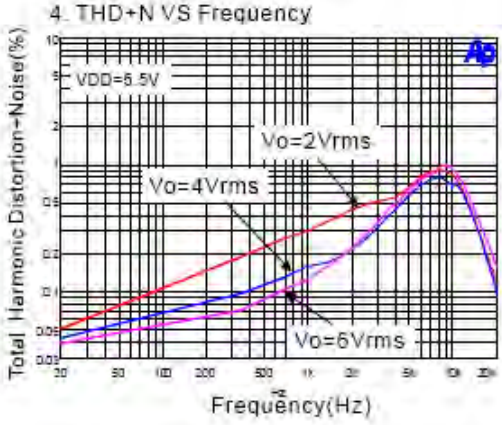

2. Total Input Power VS Output Voltage



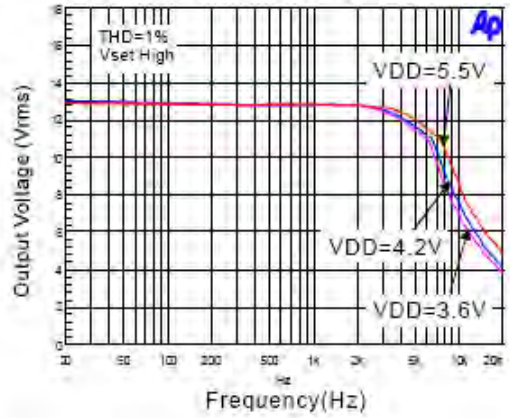

3. THD+N VS Frequency



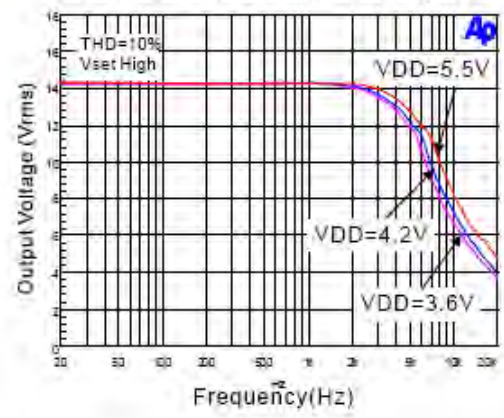

4. THD+N VS Frequency




5. Output Voltage RMS VS Frequency




6. Output Voltage RMS VS Frequency

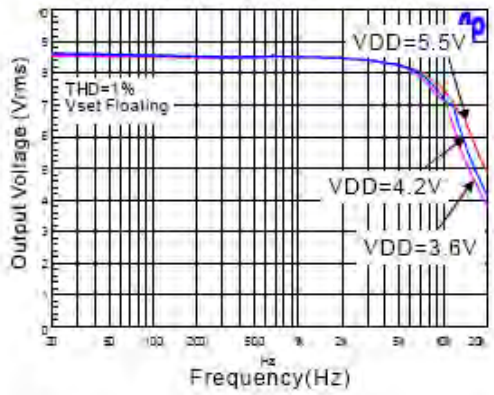




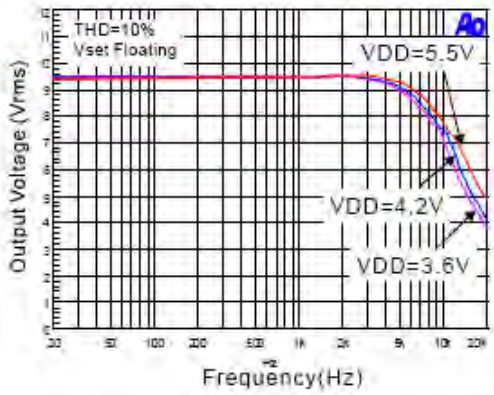
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## Typical Operating Characteristics (cont.) (@$T_A$ = +25°C, $V_{DD}$ = 5V, Gain = 18dB, unless otherwise specified.)

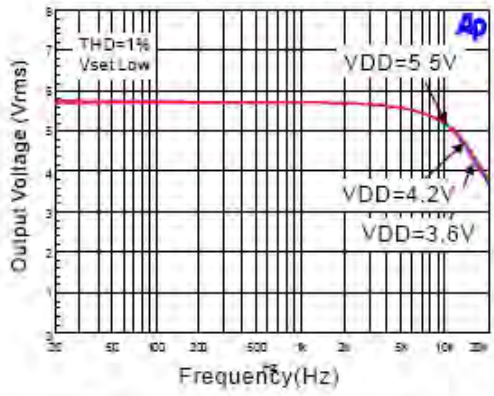
7. Output Voltage RMS VS Frequency



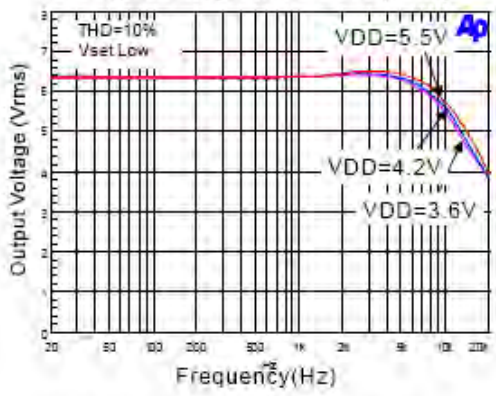

8. Output Voltage RMS VS Frequency



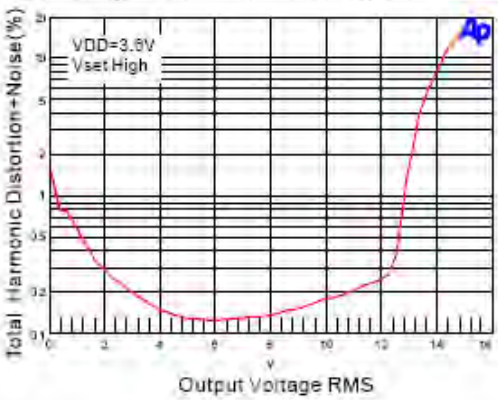

9. Output Voltage RMS VS Frequency



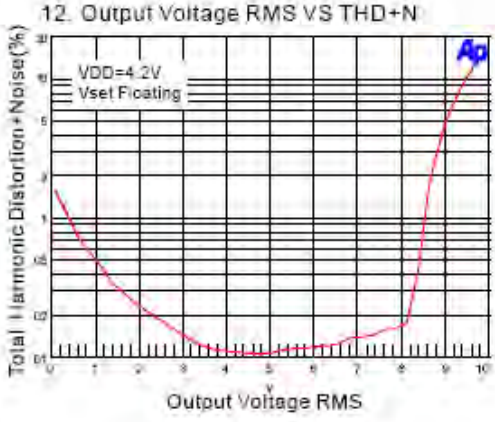

10. Output Voltage RMS VS Frequency




11. Output Voltage RMS VS THD+N




12. Output Voltage RMS VS THD+N





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## Application Information

### Select Boost Convertor Output Voltage

Customer can use $V_{SET}$ pin to set boost converor output voltage between 8V, 12V and 17.5V. $V_{SET}$ pin configuration table as below:

| $V_{SET}$ Pin Configuration | Min | Max | PVCC Voltage | Audio Amplifier Maximum Output Voltage |
|---|---|---|---|---|
| Connect to AVDD | AVDD – 0.5V | AVDD | 17.5V | $11V_{RMS}$ ($V_{PP}$ = 31.1V) |
| Floating | 1V | AVDD – 1V | 12V | $5V_{RMS}$ ($V_{PP}$ = 22.6V) |
| Connect to GND | GND | 0.5V | 8V | $5V_{RMS}$ ($V_{PP}$ = 14.1V) |

### Input Resistance ($R_I$)

The input resistors ($R_I = R_{IN} + R_{EX}$) set the gain of the amplifier according to Equation 1 when anti-saturation is inactive.

$$G = 20 \text{ Log } [12.8*R_F/(R_{IN}+R_{EX})] \text{ (dB)}$$

| $G_{SET}$ | $R_{IN}$ | $R_F$ |
|---|---|---|
| $G_{SET} = V_{DD}$ | 36.5kΩ | 122.6kΩ |
| $G_{SET}$ = Floating | 59kΩ | 100kΩ |
| $G_{SET}$ = GND | 82kΩ | 77.4kΩ |

Where $R_{IN}$ is a 77.4KΩ internal resistor, $R_{EX}$ is the external input resistor, $R_F$ is a 122.6KΩ internal resistor. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the PAM8902H to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to lower. Lower gain allows the PAM8902H to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise. In addition to these features, higher value of $R_I$ minimizes pop noise.

### Input Capacitors ($C_I$)

In the typical application, an input capacitor, $C_I$, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, $C_I$ and the minimum input impedance $R_I$ form is a high-pass filter with the corner frequency determined in the follow equation:

$$f_C = \frac{1}{2\pi R_I C_I}$$

It is important to consider the value of $C_I$ as it directl y affects the low frequency performance of the circuit. For example, when $R_I$ is 150kΩ and the specification calls for a flat bass response are down to 150Hz. Equation is reconfigured as followed:

$$C_I = \frac{1}{2\pi R_{IFC}}$$

When input resistance variation is considered, the $C_I$ is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network ($C_I$, $R_I + R_F$) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.


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## Application Information (cont.)

### Decoupling Capacitor

The PAM8902H is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes or digital hash on the line, a good low equivalent series-resistance (ESR) ceramic capacitor, typically 1µF, is placed as close as possible to the device AVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10µF or greater placed near the AVDD supply trace is recommended.

### External Schottky Diode

Use external schottky diode can get the best driving capability and efficiency. Since internal power diode has limited driving capability, only in following conditions customer can remove the external schottky diode to reduce the cost.

1. $V_{SET}$ = GND or Floating and $C_L$ less than 1µF.
2. The signal frequency less than 4KHz.
3. Haptic application (50-500Hz)

### Shutdown Operation

In order to reduce power consumption while not in use, the PAM8902H contains shutdown circuitry amplifier off when a logic low is placed on the ENA pin. By switching the ENA pin connected to GND, the PAM8902H supply current draw will be minimized in idle mode.

### Under Voltage Lock-out (UVLO)

The PAM8902H incorporates circuitry designed to detect supply voltage. When the supply voltage drops to 2.2V or below, the PAM8902H goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or ENA pin.

### Short Circuit Protection (SCP)

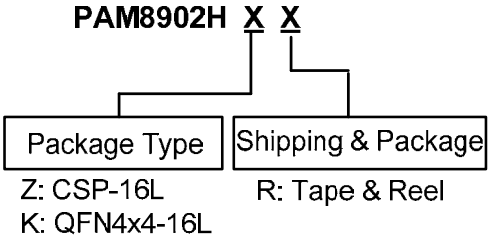
The PAM8902H has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorted or output-to-GND shorted occurs. When a short circuit occurs, the dev ice goes into a latch state and must be reset by cycling the voltage on the ENA pin to a logic low and then back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

### Over Temperature Protection (OTP)

Thermal protection on the PAM8902H prevents the device from damage when the internal die temperature exceeds +150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled, in this condition both OUT+ and OUT- will become high impedance. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 30°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.


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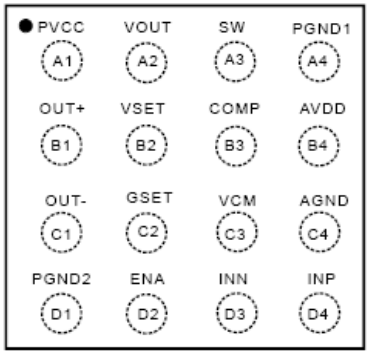
## Ordering Information




| Part Number | Part Marking | Package Type | Standard Package |
|---|---|---|---|
| PAM8902HZER | BT<br>YW | CSP-16L | 3000 Units/Tape&Reel |
| PAM8902HKER | P8902H<br>XXXYW | QFN4x4-16L | 3000 Units/Tape&Reel |

## Marking Information

16 Ball CSP
Top View

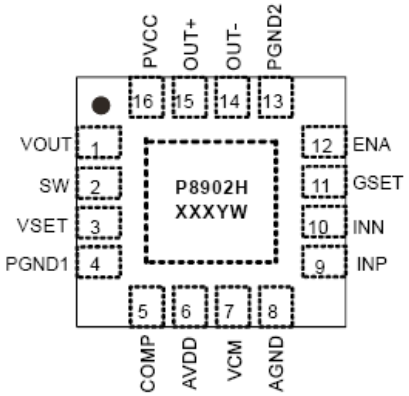



**Marking**

BT
YW

BT: Product Code of PAM8902H
Y: Year
W: Week

Top View
QFN 4X4 16L



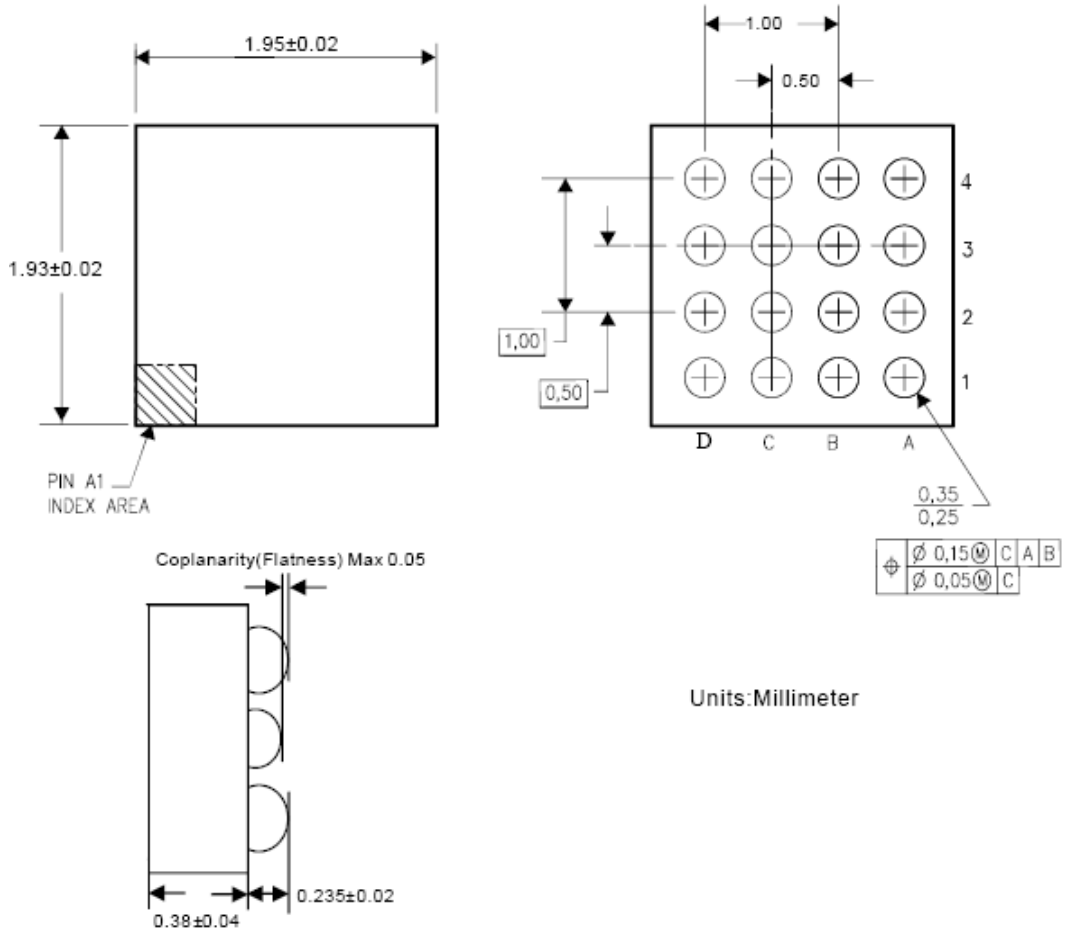

Y: Year
W: Week
X: Internal Code

● : Pin 1 Indicator


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## Package Outline Dimensions (All dimensions in mm.)

**CSP-16**

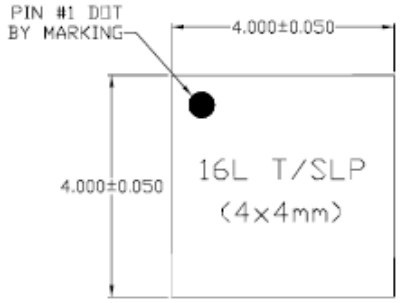




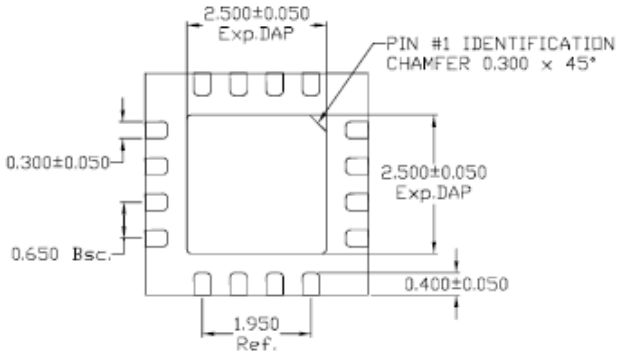
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## Package Outline Dimensions (All dimensions in mm.)

**QFN4x4-16**



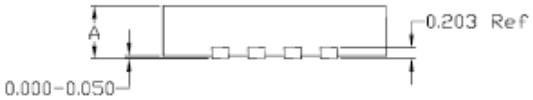

TOP VIEW




BOTTOM VIEW

NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS.

| | | TSLP | SLP |
|---|---|---|---|
| A | MAX. | 0.800 | 0.900 |
| | NOM. | 0.750 | 0.850 |
| | MIN. | 0.700 | 0.800 |




SIDE VIEW


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A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

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