Green-Mode PWM Controller with Programmable OLP Delay Time and Integrated Protections

REV: 01

General Description

The LD7530M/LD7530N are specifically designed for the low total system cost by integrating many functions and protections in a tiny SOT-26 package which usually need a lot of extra components or circuits on the general designs.

Furthermore, the programmable OLP delay time function is to reduce the circuit complexity and thus helps the power circuit designers to easily deal with the peak load design by using minimum component cost and developing time.

And to satisfy different designs, 2 versions of OVP levels are implemented as ---

- LD7530M --- 28.0V ± 2.0V.
- LD7530N --- 21.0V ± 2.0V.

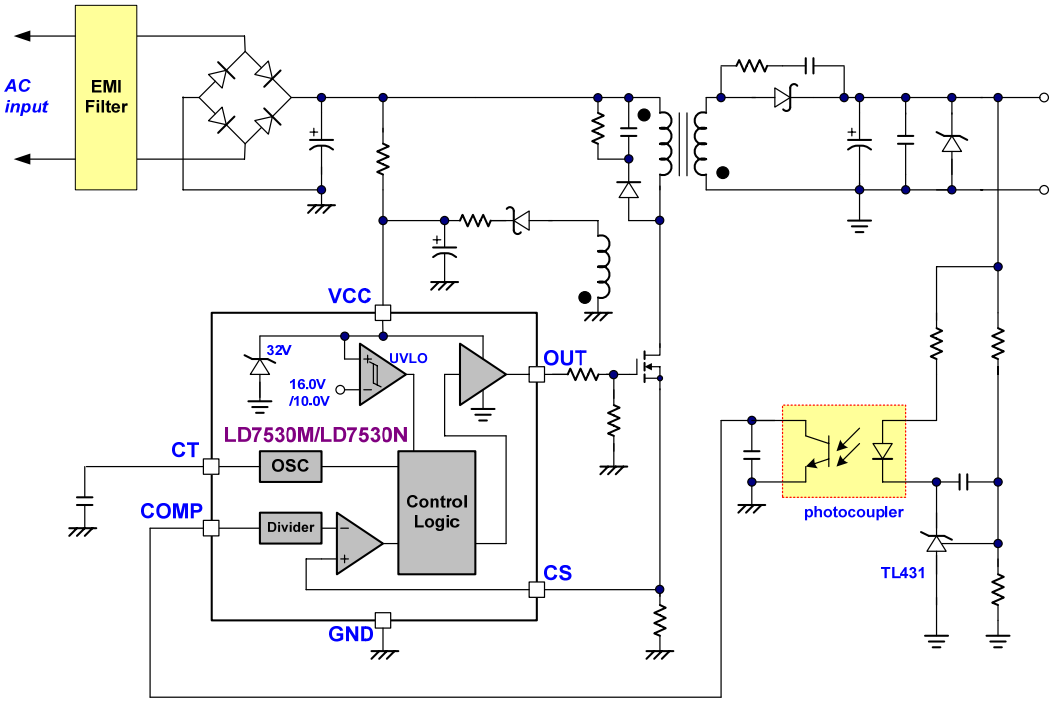
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<30μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- OLP (Over Load Protection) and programmable timer
- 300mA Driving Capability

Applications

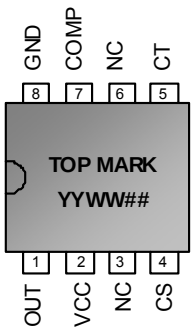
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application

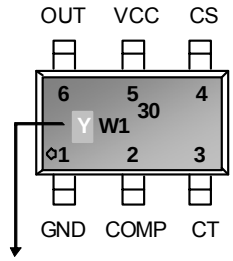


Pin Configuration (LD7530M)

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)

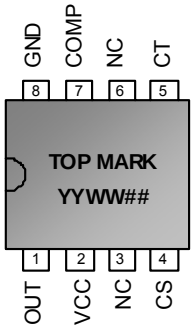


Y The PB free package is identified in embossed font, while Green compound package in normal print

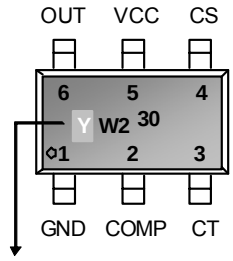
YY, Y: Year code (D: 2004, E: 2005…..)
WW, W: Week code
1 : LD75..(M) (Product family code)
: Production code

Pin Configuration (LD7530N)

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



Y The PB free package is identified in embossed font, while Green compound package in normal print

YY, Y: Year code (D: 2004, E: 2005…..)
WW, W: Week code
2 : LD75..(N) (Product family code)
: Production code

Ordering Information

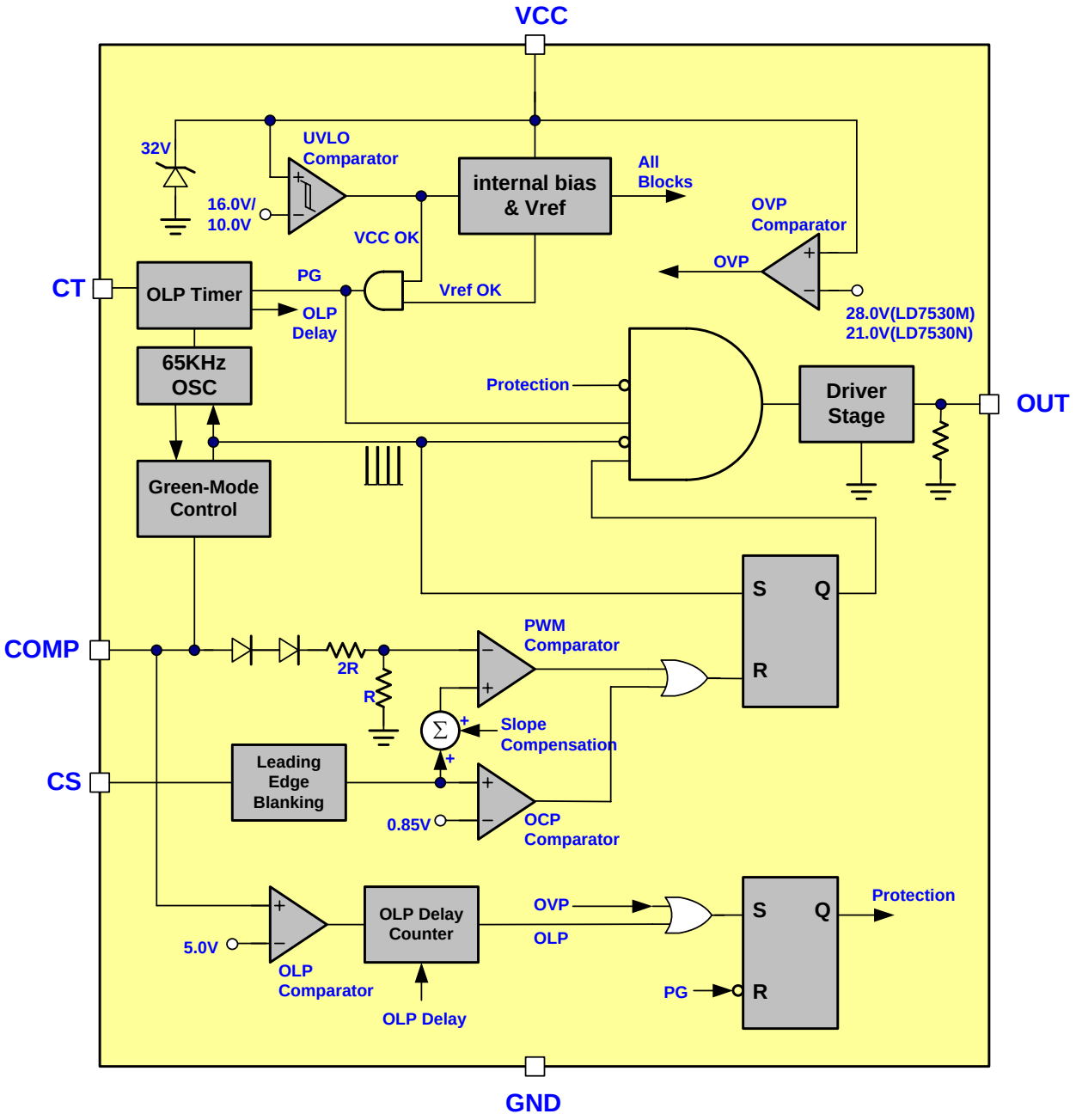
Part number	Package		TOP MARK	Shipping
LD7530MGL	SOT-26	Green Package	YW1/30	3000 /tape & reel
LD7530MPL	SOT-26	PB free	YW1/30	3000 /tape & reel
LD7530MPN	DIP-8	PB free	LD7530MPN	3600 /tube /Carton
LD7530NGL	SOT-26	Green Package	YW2/30	3000 /tape & reel
LD7530NPL	SOT-26	PB free	YW2/30	3000 /tape & reel
LD7530NPN	DIP-8	PB free	LD7530NPN	3600 /tube /Carton

Note: The LD7530M/N are ROHS compliant/ Green Package.

Pin Descriptions

PIN (SOT-26)	PIN (DIP-8)	NAME	FUNCTION
1	8	GND	Ground
2	7	COMP	Voltage feedback pin (same as the COMP pin in UC384X), By connecting a photo-coupler to close the control loop and achieve the regulation.
3	5	CT	This pin is to program the delay timer. By connecting a capacitor to ground to set the OLP delay time.
4	4	CS	Current sense pin, connect to sense the MOSFET current
5	2	VCC	Supply voltage pin
6	1	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
COMP, CT, CS	-0.3 ~7V
Junction Temperature	150°C
Operating Ambient Temperature	-20°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26)	250°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	300mA

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc (LD7530M)	11	25	V
Supply Voltage Vcc (LD7530N)	11	18	V
CT Value	0.047	0.1	μF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			8	30	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.0	3.0	mA
	V_{COMP}=3V		2.5		mA
	Protection tripped (OLP, OVP)		0.5		mA
UVLO (off)		8.5	10.0	11.0	V
UVLO (on)		14.5	16.0	17.5	V
OVP Level	LD7530M	26.0	28.0	30.0	V
	LD7530N	19.0	21.0	23.0	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		1.5	3.0	mA
Open Loop Voltage	COMP pin open		6.0		V
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.78	0.85	0.92	V
Leading Edge Blanking Time			200		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency		59	65	71	KHz
Green Mode Frequency			20		KHz
Temp. Stability	(-40°C ~105°C)			6	%
Voltage Stability	(VCC=11V-25V)			2	%
OLP Timer (CT pin)					
Frequency	CT=0.1μF		100		Hz
	CT=0.047μF		200		Hz
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF		50	250	nS
Falling Time	Load Capacitance=1000pF		30	150	nS
OLP (Over Load Protection)					
OLP Trip Level	Vcomp(OLP)		5.0		V
OLP Delay Time	CT=0.047μF		50		mS

Typical Performance Characteristics

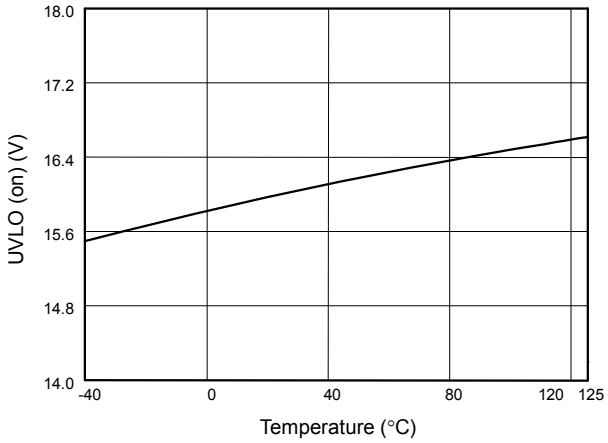


Fig. 1 UVLO (on) vs. Temperature

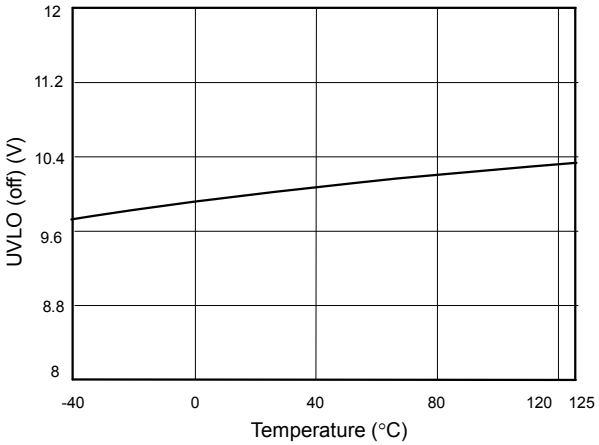


Fig. 2 UVLO (off) vs. Temperature

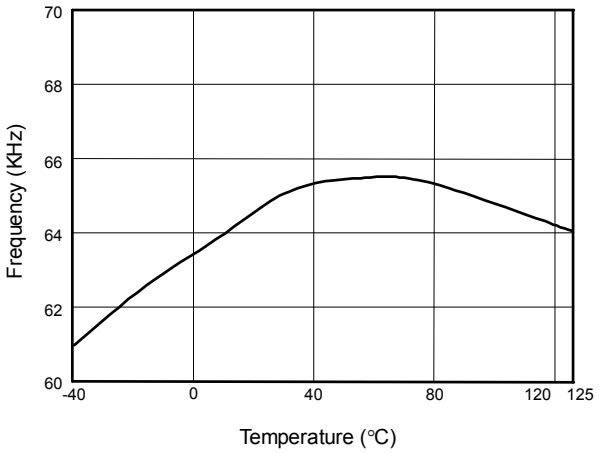


Fig. 3 Frequency vs. Temperature

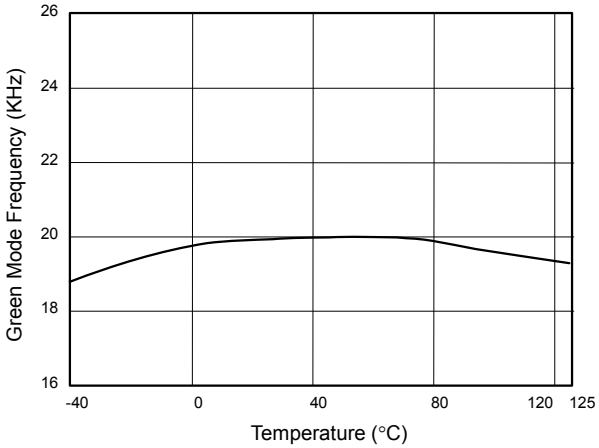


Fig. 4 Green Mode Frequency vs. Temperature

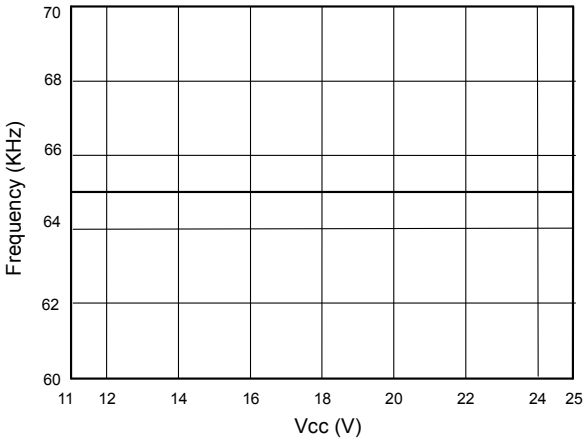


Fig. 5 Frequency vs. Vcc

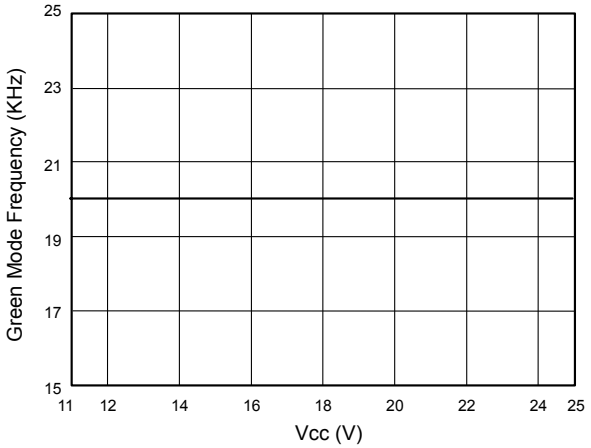


Fig. 6 Green Mode Frequency vs. Vcc

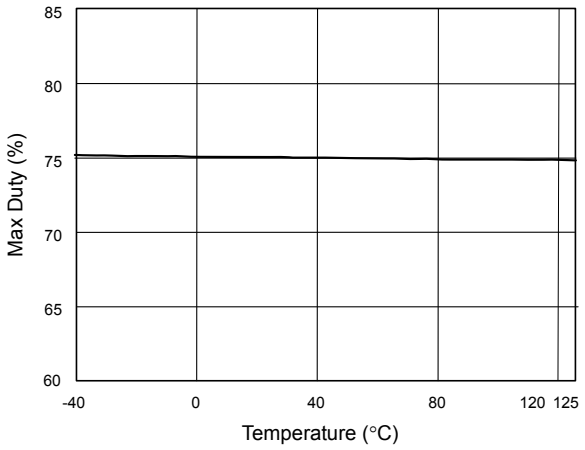


Fig. 7 Max Duty vs. Temperature

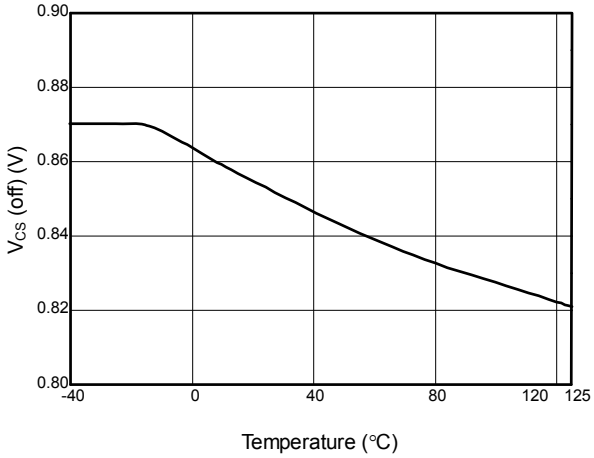


Fig. 8 V_{CS} (off) vs. Temperature

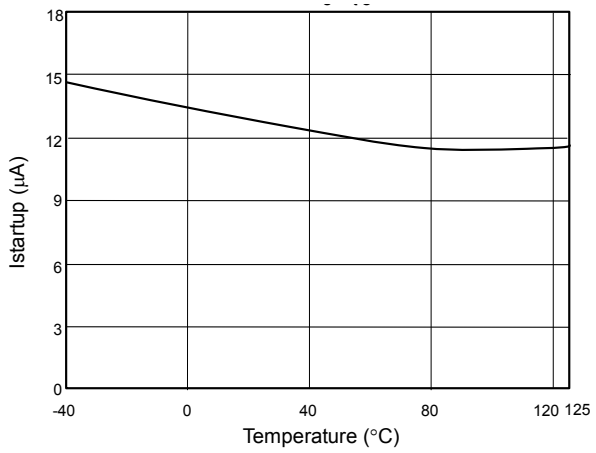


Fig. 9 Startup Current (Istartup) vs. Temperature

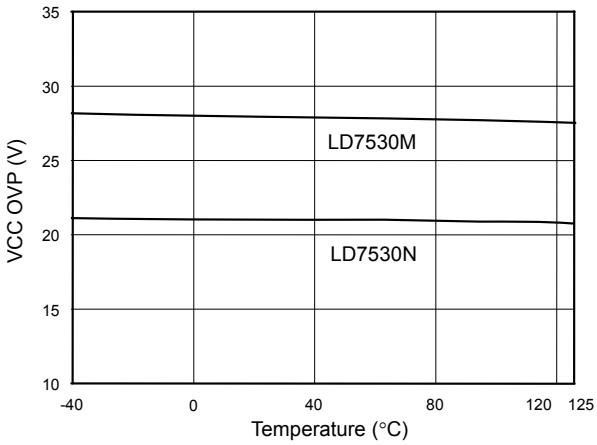


Fig. 10 VCC OVP vs. Temperature

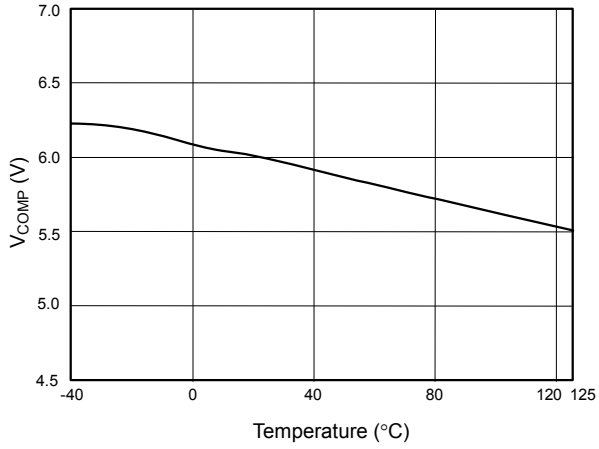


Fig. 11 V_{COMP} open loop voltage vs. Temperature

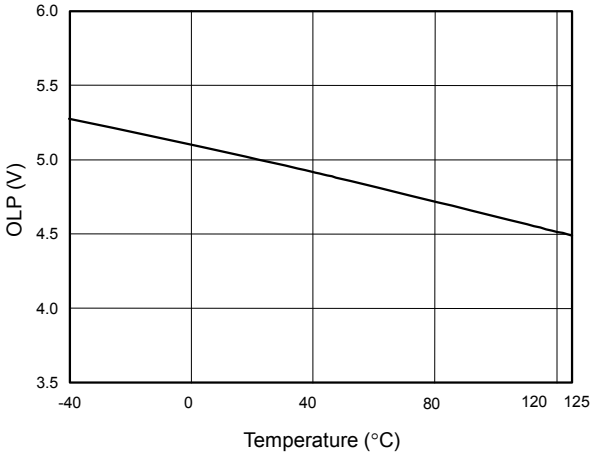


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7530M/LD7530Nmeet the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7530M/LD7530N PWM controllers and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 10.0V, respectively.

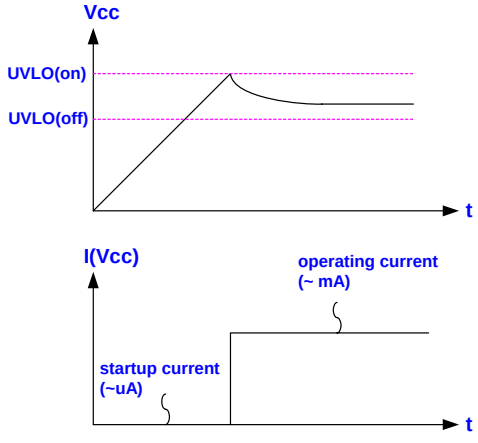


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7530M/LD7530N Vcc is shown in Fig. 14. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7530M/LD7530N to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7530M/LD7530N and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7530M/LD7530N is only 30μA.

If a higher resistance value of the R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

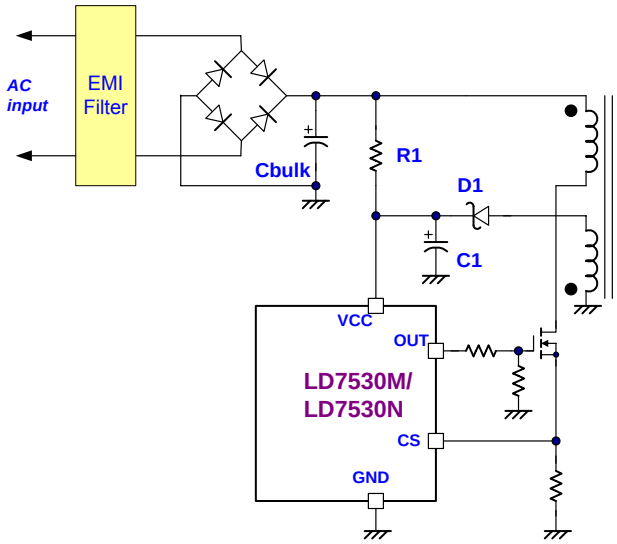


Fig. 14

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD7530M/LD7530N detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

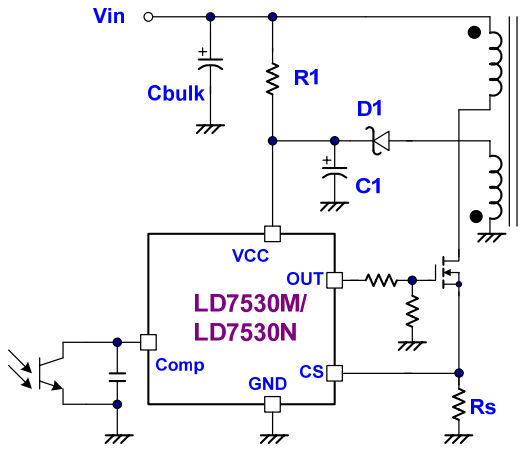


Fig. 15

A 200nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 200nS and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter (as shown in the figure16).

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in figure 17) for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7530M/LD7530N is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7530M/LD7530N. Similar to UC3842, the LD7530M/LD7530N would carry 2 diodes voltage offset at the stage to feed the voltage divider at the ratio of 1/3, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

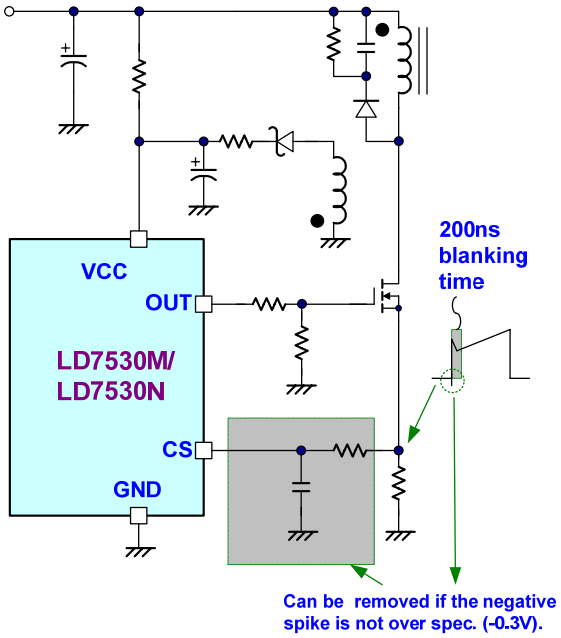


Fig. 16

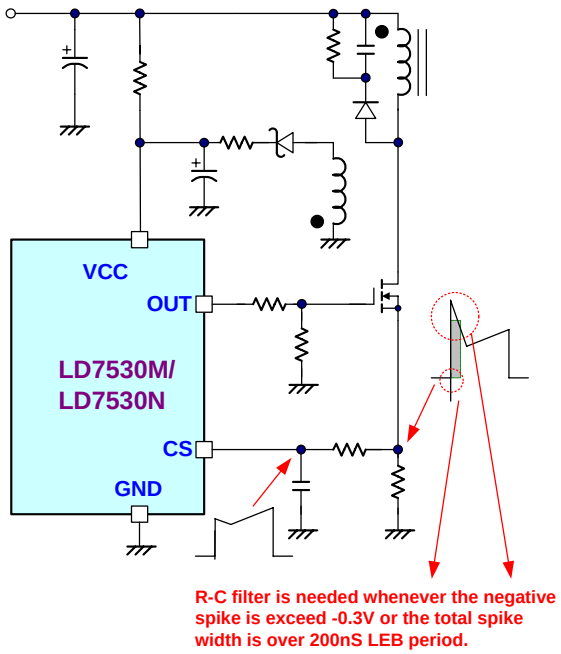


Fig. 17

Oscillator and Switching Frequency

The switching frequency of LD7530M/LD7530N is fixed as 65 KHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7530M/LD7530N since it has integrated it already.

On/Off Control

The LD7530M/LD7530N can be turned off by pulling COMP pin lower than 1.2V. The gate output pin of the LD7530M/LD7530N will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

What LD7530M/LD7530N use to implement the power-saving operation is Leadtrend Technology’s own IP. By using this dual-oscillator control, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 30V. To prevent the V_{GS} from the fault condition, LD7530M/LD7530N are implemented an OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on).

The Vcc OVP function in LD7530M/LD7530N is an auto-recovery type protection. If the OVP condition, usually caused by the feedback loop opened, is not released, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc is working as a hiccup mode. The figure 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output will automatically return to the normal operation.

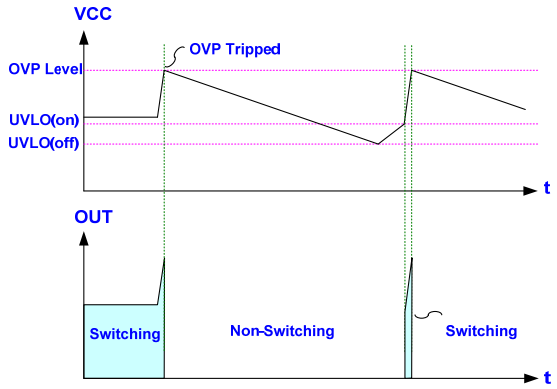


Fig. 18

Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is implemented in the LD7530M/LD7530N. The figure 19 shows the waveforms of the OLP operation. In this case, the feedback system will force the voltage loop proceed toward the saturation and then pull up the voltage on COMP pin (V_{COMP}). Whenever the V_{COMP} trips up to the OLP threshold 5V and stays longer than the OLP delay time, the protection will activate and then turn off the gate output to stop the switching of power circuit. The OLP delay time, set by CT pin, is to prevent the false trigger from the power-on and turn-off transient. Higher CT value will generate longer OLP delay time. For the recommended CT value, the OLP delay time is around 90mS when CT=0.1μF and will be around 50mS if CT=0.047μF.

By such protection mechanism, the average input power can be reduced to very low level so that the component temperature and stress can be controlled within the safe operating area.

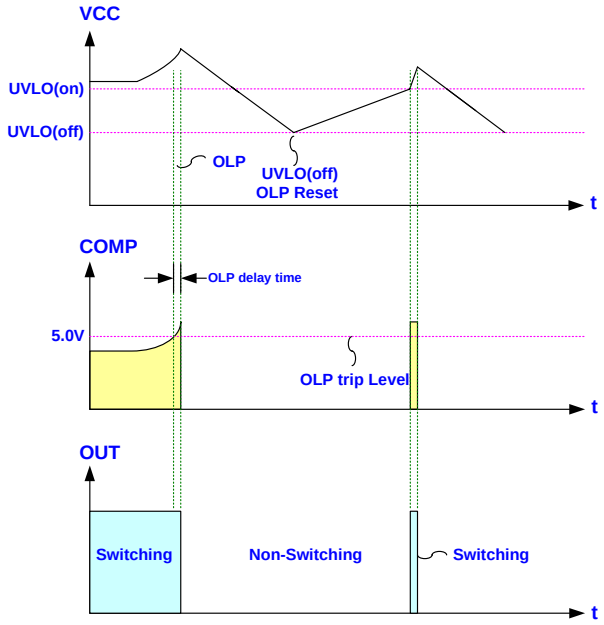
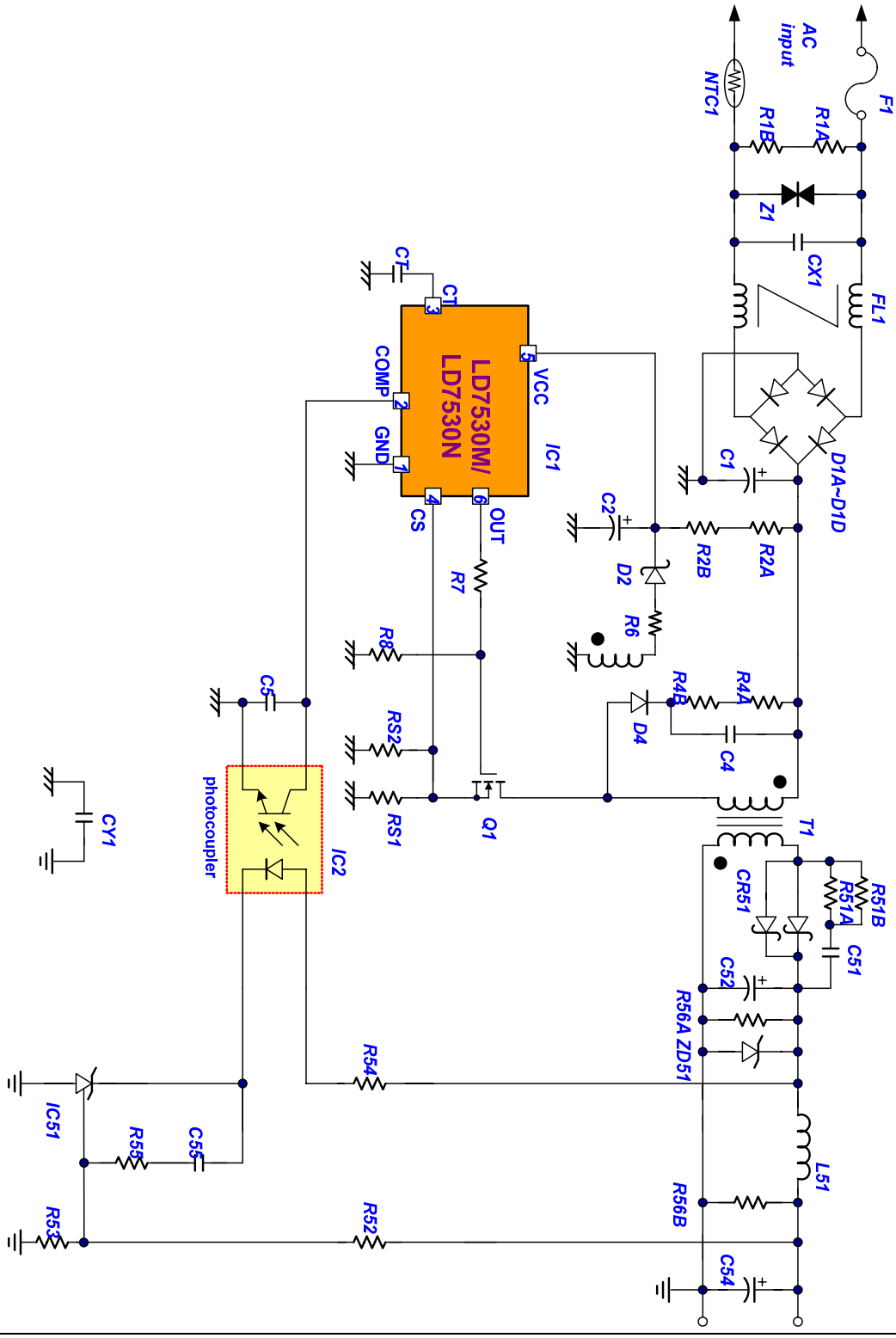

VCC
UVLO(on)
UVLO(off)
OLP
UVLO(off)
OLP Reset
t
COMP
OLP delay time
5.0V
OLP trip Level
t
OUT
Switching
Non-Switching
Switching
t

Fig. 19

Reference Application Circuit --- 10W (5V/2A) Adapter

Schematic



Reference Application Circuit --- 10W (5V/2A) Adapter

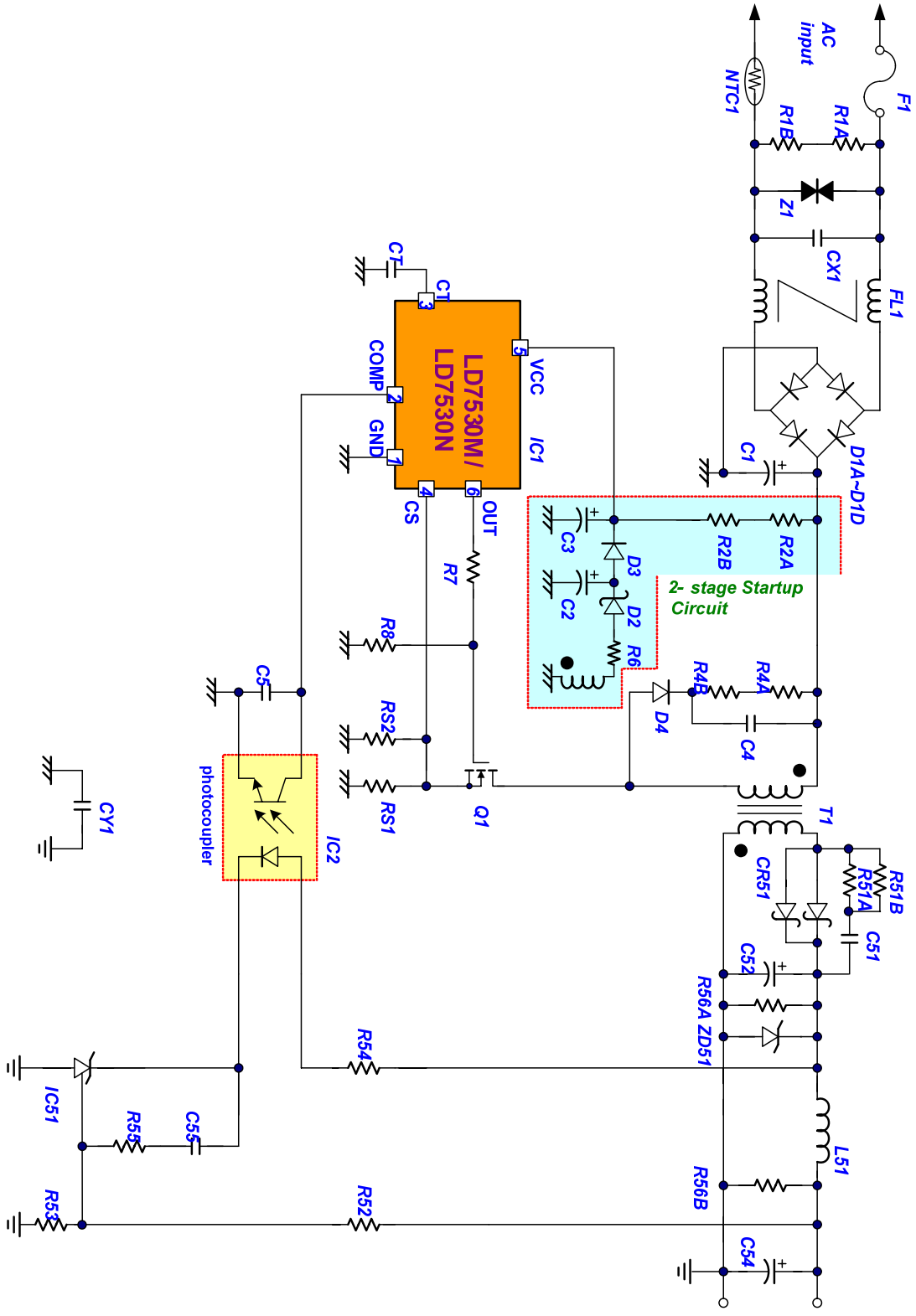
BOM

P/N	Component Value	Original
R1A	N/A	
R1B	N/A	
R2A	750KΩ, 1206	
R2B	750KΩ, 1206	
R4A	39KΩ, 1206	
R4B	39KΩ, 1206	
R6	10Ω, 1206	
R7	10Ω, 1206	
R8	10KΩ, 1206	
RS1	2.70Ω, 1206, 1%	
RS2	2.70Ω, 1206, 1%	
R51A	100Ω, 1206	
R51B	100Ω, 1206	
R52	2.49KΩ, 0805, 1%	
R53	2.49KΩ, 0805, 1%	
R54	220Ω, 0805	
R55	10KΩ, 0805	
R56A	510Ω, 1206	
R56B	N/A	
NTC1	08SP005	
FL1	20mH	UU9.8
T1	EI-22	
L51	2.7μH	

P/N	Component Value	Note
C1	22μF, 400V	L-tec
C2	10μF, 50V	
C4	1000pF, 1000V, 1206	Holystone
C5	0.01μF, 16V, 0805	
C51	1000pF, 50V, 0805	
C52	1000μF, 10V	L-tec
C54	470μF, 10V	L-tec
C55	0.01μF, 16V, 0805	
CT	0.047μF, 16V, 0805	X7R
CX1	0.1μF	X-cap
CY1	2200pF	Y-cap
D1A	1N4007	
D1B	1N4007	
D1C	1N4007	
D1D	1N4007	
D2	PS102R	
D4	1N4007	
Q1	2N60B	600V/2A
CR51	SB540	
ZD51	6V2C	
IC1	LD7530M/LD7530N	SOT-26
IC2	EL817B	
IC51	TL431	1%
F1	250V, 1A	
Z1	N/A	

Reference Application Circuit #2 --- 10W Adapter with 2-Stage Startup Circuit

Pin < 0.25W when Pout = 0W



Reference Application Circuit #2 --- 10W Adapter with 2-Stage Startup Circuit

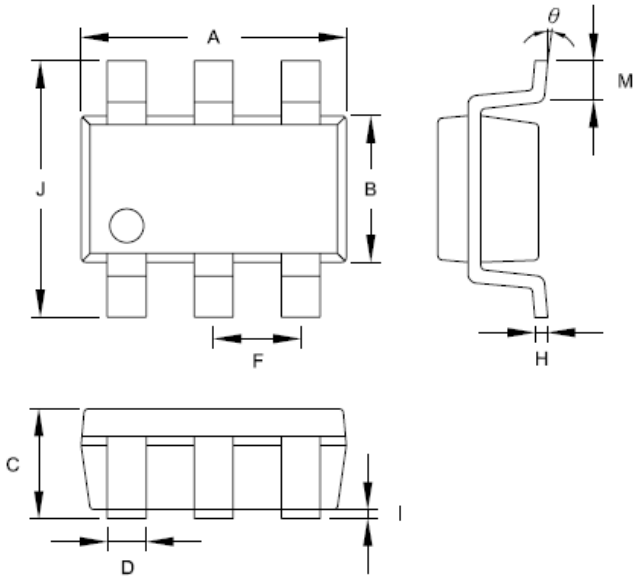
BOM

P/N	Component Value	Original
R1A	N/A	
R1B	N/A	
R2A	2.2MΩ, 1206	
R2B	2.2MΩ, 1206	
R4A	39KΩ, 1206	
R4B	39KΩ, 1206	
R6	2.2Ω, 1206	
R7	10Ω, 1206	
R8	10KΩ, 1206	
RS1	2.70Ω, 1206, 1%	
RS2	2.70Ω, 1206, 1%	
R51A	100Ω, 1206	
R51B	100Ω, 1206	
R52	2.49KΩ, 0805, 1%	
R53	2.49KΩ, 0805, 1%	
R54	220Ω, 0805	
R55	10KΩ, 0805	
R56A	1KΩ, 1206	
R56B	N/A	
NTC1	5Ω, 3A	08SP005
FL1	20mH	UU9.8
T1	EI-22	
L51	2.7μH	

P/N	Component Value	Note
C1	22μF, 400V	L-tec
C2	10μF, 50V	L-tec
C3	2.2μF, 50V	
C4	1000pF, 1000V, 1206	Holystone
C5	0.01μF, 16V, 0805	
C51	1000pF, 50V, 0805	
C52	1000μF, 10V	L-tec
C54	470μF, 10V	L-tec
C55	0.01μF, 16V, 0805	
CT	0.047μF, 16V, 0805	X7R
CX1	0.1μF	X-cap
CY1	2200pF	Y-cap
D1A	1N4007	
D1B	1N4007	
D1C	1N4007	
D1D	1N4007	
D2	PS102R	
D3	1N4148	
D4	1N4007	
Q1	2N60B	600V/2A
CR51	SB540	
ZD51	6V2C	
IC1	LD7530M/LD7530N	SOT-26
IC2	EL817B	
IC51	TL431	1%
F1	250V, 1A	
Z1	N/A	

Package Information

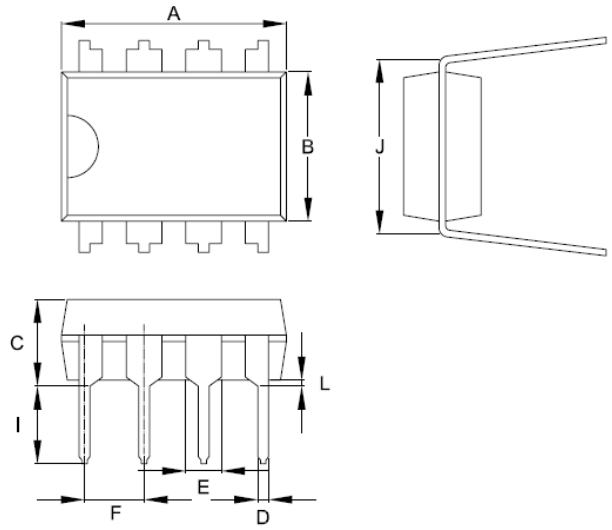
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.290	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	1/30/08	Original Specification.
00a	4/11/08	Revise application information (LEB)
01	6/4/08	Top Marking