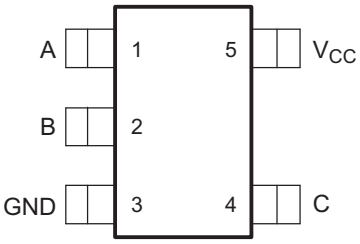
# SINGLE BILATERAL ANALOG SWITCH

**Check for Samples: SN74LVC1G66**

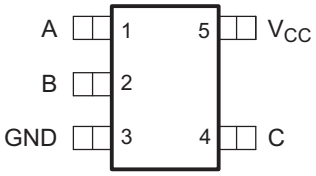
## FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **1.65-V to 5.5-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max $t_{pd}$ of 0.8 ns at 3.3 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed, Typically 0.5 ns ($V_{CC}$ = 3 V, $C_L$ = 50 pF)**
- **Low On-State Resistance, Typically ≠5.5 Ω ($V_{CC}$ = 4.5 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

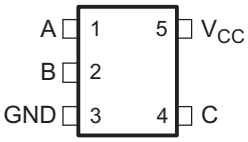
**DBV PACKAGE**
**(TOP VIEW)**



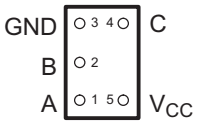

**DCK PACKAGE**
**(TOP VIEW)**



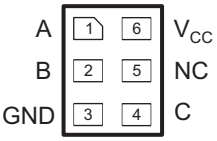

**DRL PACKAGE**
**(TOP VIEW)**



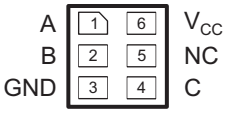

**YZP PACKAGE**
**(BOTTOM VIEW)**




**DRY PACKAGE**
**(TOP VIEW)**




**DSF PACKAGE**
**(TOP VIEW)**




See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This single analog switch is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## Table 1. ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING(2) |
|---|---|---|---|---|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74LVC1G66YZPR | _ _ _C6_ |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74LVC1G66DBVR | C66_ |
| | | Reel of 250 | SN74LVC1G66DBVT | |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74LVC1G66DCKR | C6_ |
| | | Reel of 250 | SN74LVC1G66DCKT | |
| | | Jumbo Reel of 10000 | SN74LVC1G66DCKJ | |
| | SOT (SOT-553) – DRL | Reel of 4000 | SN74LVC1G66DRLR | |
| | QFN – DRY | Reel of 5000 | SN74LVC1G66DRYR | C6 |
| | µQFN – DSF | Reel of 5000 | SN74LVC1G66DSFR | |

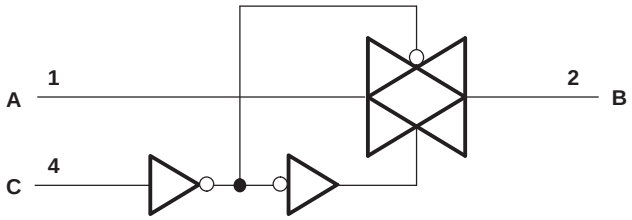
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

## FUNCTION TABLE

| CONTROL INPUT (C) | SWITCH |
|---|---|
| L | OFF |
| H | ON |

## LOGIC DIAGRAM (POSITIVE LOGIC)





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## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) (3) | | –0.5 | 6.5 | V |
| $V_{I/O}$ | Switch I/O voltage range(2) (3) (4) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Control input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{IOK}$ | I/O port diode current | $V_{I/O}$ < 0 or $V_{I/O}$ > $V_{CC}$ | | ±50 | mA |
| $I_T$ | On-state switch current | $V_{I/O}$ < 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(5) | DBV package | | 206 | °C/W |
| | | DCK package | | 252 | |
| | | DRL package | | 142 | |
| | | YZP package | | 132 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

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## Recommended Operating Conditions(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_{I/O}$ | I/O port voltage | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage, control input | $V_{CC}$ = 1.65 V to 1.95 V | $V_{CC}$ × 0.65 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage, control input | $V_{CC}$ = 1.65 V to 1.95 V | | $V_{CC}$ × 0.35 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Control input voltage | | 0 | 5.5 | V |
| Δt/Δv | Input transition rise/fall time | $V_{CC}$ = 1.65 V to 1.95 V | | 20 | ns/V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 20 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 10 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 10 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $r_{on}$ | On-state switch resistance | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$ (see Figure 1 and Figure 2) | $I_S$ = 4 mA | 1.65 V | | 12 | 30 | Ω |
| | | | $I_S$ = 8 mA | 2.3 V | | 9 | 20 | |
| | | | $I_S$ = 24 mA | 3 V | | 7.5 | 15 | |
| | | | $I_S$ = 32 mA | 4.5 V | | 5.5 | 10 | |
| $r_{on(p)}$ | Peak on resistance | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$ (see Figure 1 and Figure 2) | $I_S$ = 4 mA | 1.65 V | | 74.5 | 120 | Ω |
| | | | $I_S$ = 8 mA | 2.3 V | | 20 | 30 | |
| | | | $I_S$ = 24 mA | 3 V | | 11.5 | 20 | |
| | | | $I_S$ = 32 mA | 4.5 V | | 7.5 | 15 | |
| $I_{S(off)}$ | Off-state switch leakage current | $V_I$ = $V_{CC}$ and $V_O$ = GND or $V_I$ = GND and $V_O$ = $V_{CC}$, $V_C$ = $V_{IL}$ (see Figure 3) | | 5.5 V | | | ±1 | μA |
| | | | | | | | ±0.1(1) | |
| $I_{S(on)}$ | On-state switch leakage current | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$, $V_O$ = Open (see Figure 4) | | 5.5 V | | | ±1 | μA |
| | | | | | | | ±0.1(1) | |
| $I_I$ | Control input current | $V_C$ = $V_{CC}$ or GND | | 5.5 V | | | ±1 | μA |
| | | | | | | | ±0.1(1) | |
| $I_{CC}$ | Supply current | $V_C$ = $V_{CC}$ or GND | | 5.5 V | | | 10 | μA |
| | | | | | | | 1(1) | |
| $ΔI_{CC}$ | Supply current change | $V_C$ = $V_{CC}$ – 0.6 V | | 5.5 V | | | 500 | μA |
| $C_{ic}$ | Control input capacitance | | | 5 V | | 2 | | pF |
| $C_{io(off)}$ | Switch input/output capacitance | | | 5 V | | 6 | | pF |
| $C_{io(on)}$ | Switch input/output capacitance | | | 5 V | | 13 | | pF |

(1) $T_A$ = 25°C


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## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ (1) | A or B | B or A | | 2 | | 1.2 | | 0.8 | | 0.6 | ns |
| $t_{en}$ (2) | C | A or B | 2.5 | 12 | 1.9 | 6.5 | 1.8 | 5 | 1.5 | 4.2 | ns |
| $t_{dis}$ (3) | C | A or B | 2.2 | 10 | 1.4 | 6.9 | 2 | 6.5 | 1.4 | 5 | ns |

(1) $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
(3) $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

## Analog Switch Characteristics

$T_A$ = 25°C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| Frequency response (1) (switch ON) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = sine wave (see Figure 6) | 1.65 V | 35 | MHz |
| | | | | 2.3 V | 120 | |
| | | | | 3 V | 175 | |
| | | | | 4.5 V | 195 | |
| | | | $C_L$ = 5 pF, $R_L$ = 50 Ω, $f_{in}$ = sine wave (see Figure 6) | 1.65 V | >300 | |
| | | | | 2.3 V | >300 | |
| | | | | 3 V | >300 | |
| | | | | 4.5 V | >300 | |
| Crosstalk (control input to signal output) | C | A or B | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (square wave) (see Figure 7) | 1.65 V | 35 | mV |
| | | | | 2.3 V | 50 | |
| | | | | 3 V | 70 | |
| | | | | 4.5 V | 100 | |
| Feedthrough attenuation (2) (switch OFF) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (sine wave) (see Figure 8) | 1.65 V | –58 | dB |
| | | | | 2.3 V | –58 | |
| | | | | 3 V | –58 | |
| | | | | 4.5 V | –58 | |
| | | | $C_L$ = 5 pF, $R_L$ = 50 Ω, $f_{in}$ = 1 MHz (sine wave) (see Figure 8) | 1.65 V | –42 | |
| | | | | 2.3 V | –42 | |
| | | | | 3 V | –42 | |
| | | | | 4.5 V | –42 | |
| Sine-wave distortion | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kHz (sine wave) (see Figure 9) | 1.65 V | 0.1 | % |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |
| | | | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 10 kHz (sine wave) (see Figure 9) | 1.65 V | 0.15 | |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |

(1) Adjust $f_{in}$ voltage to obtain 0 dBm at output. Increase $f_{in}$ frequency until dB meter reads –3 dB.
(2) Adjust $f_{in}$ voltage to obtain 0 dBm at input.

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## Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 8 | 9 | 9 | 11 | pF |


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## PARAMETER MEASUREMENT INFORMATION

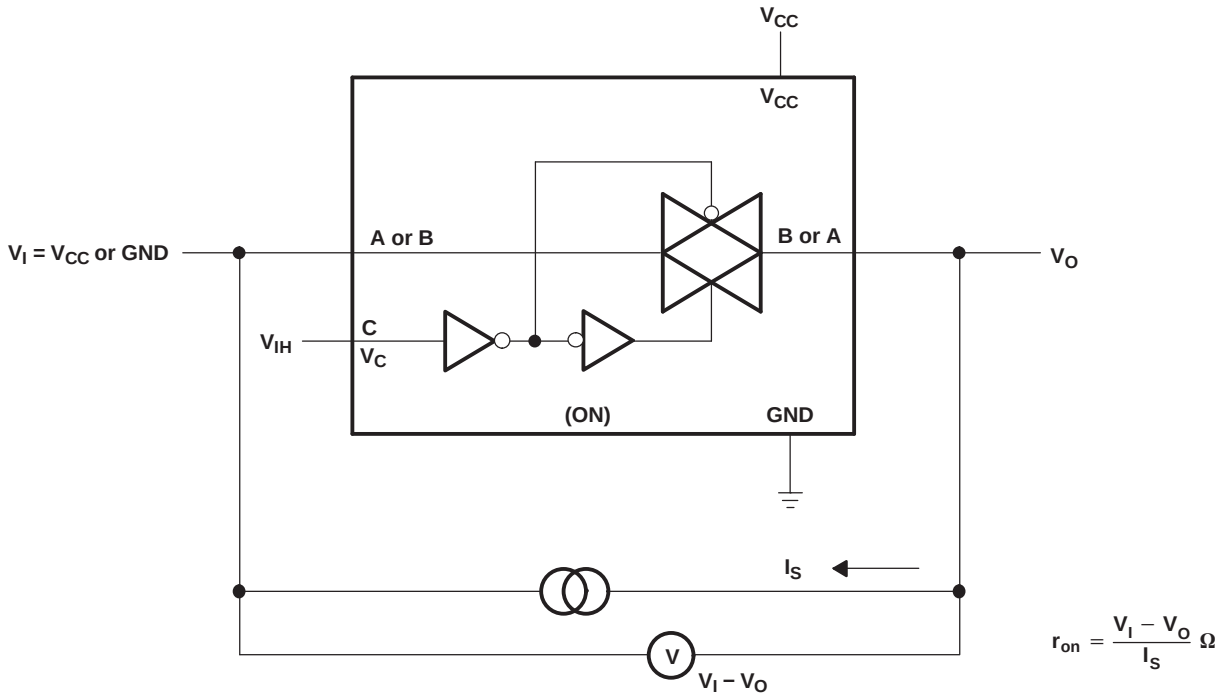



**Figure 1. On-State Resistance Test Circuit**

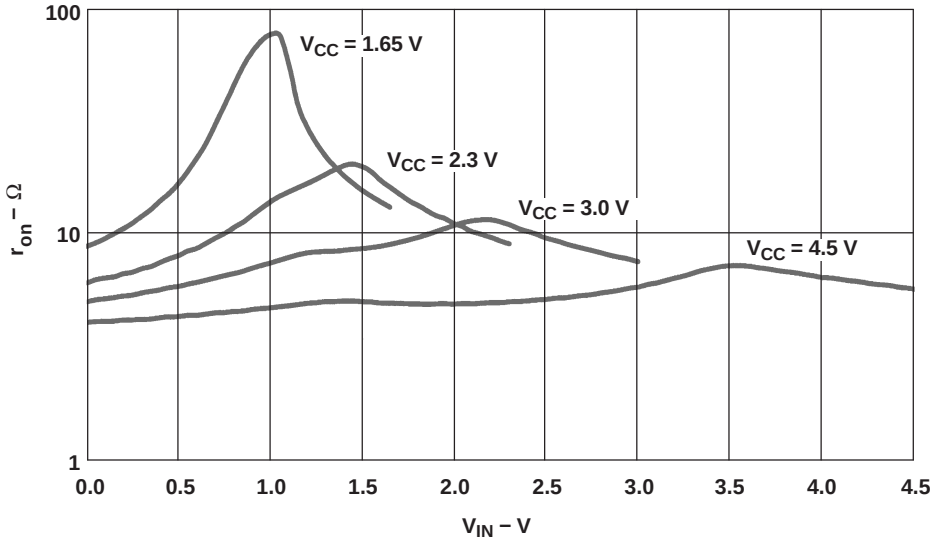



**Figure 2. Typical $r_{on}$ as a Function of Input Voltage ($V_I$) for $V_I$ = 0 to $V_{CC}$**

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## PARAMETER MEASUREMENT INFORMATION

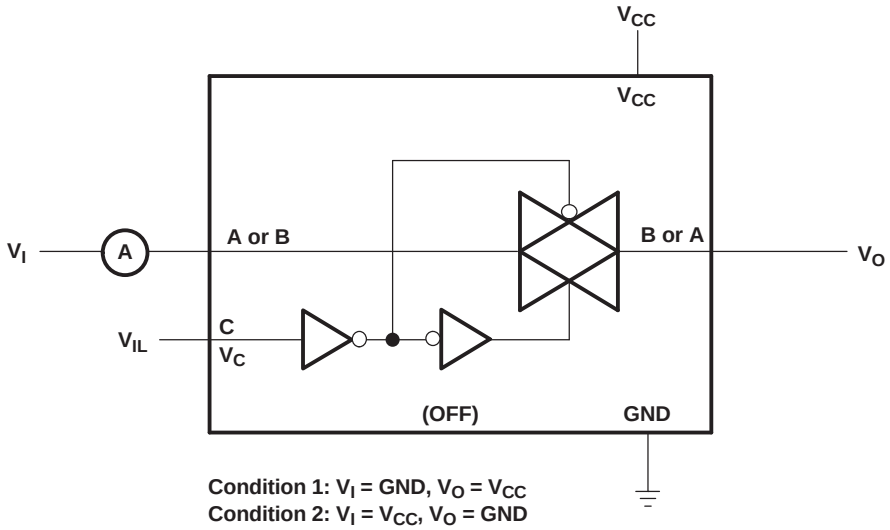



**Figure 3. Off-State Switch Leakage-Current Test Circuit**

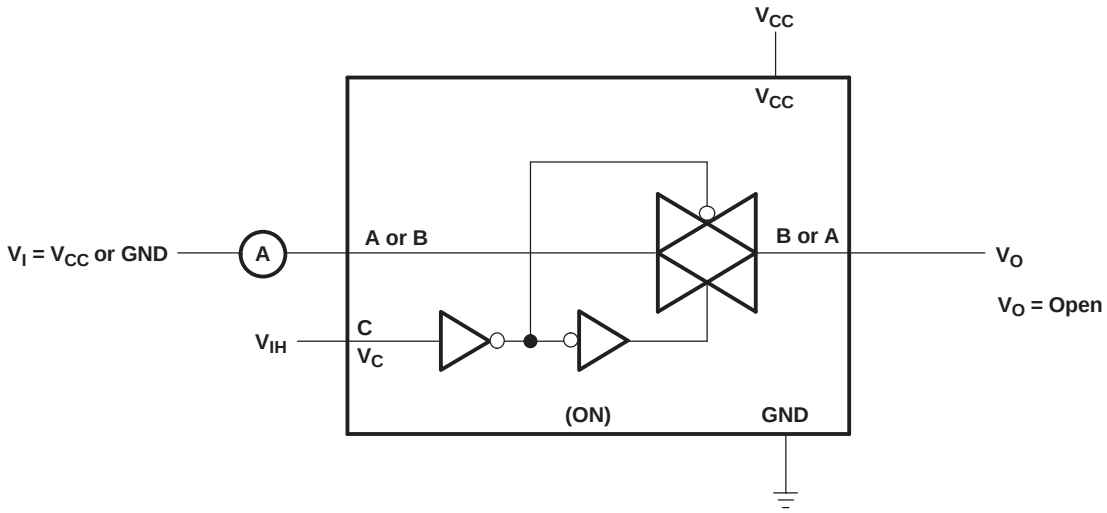
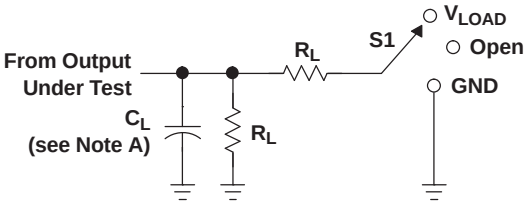



**Figure 4. On-State Switch Leakage-Current Test Circuit**


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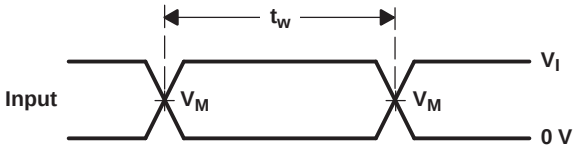
## PARAMETER MEASUREMENT INFORMATION



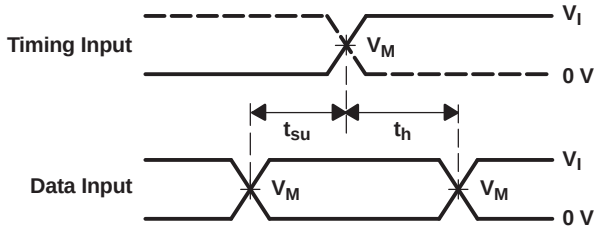

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

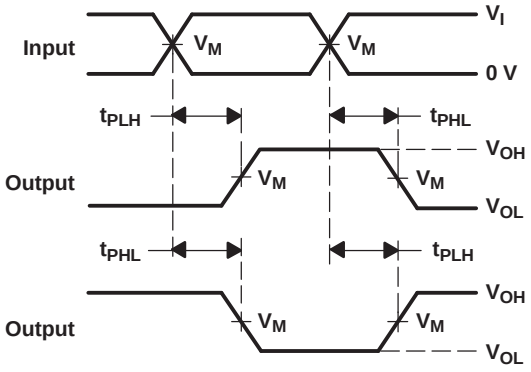
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



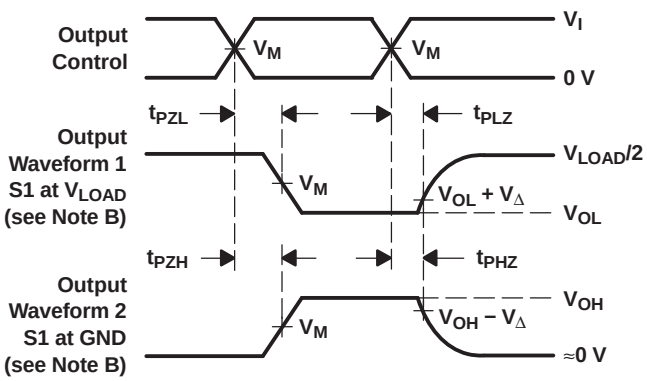

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 5. Load Circuit and Voltage Waveforms**

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## PARAMETER MEASUREMENT INFORMATION

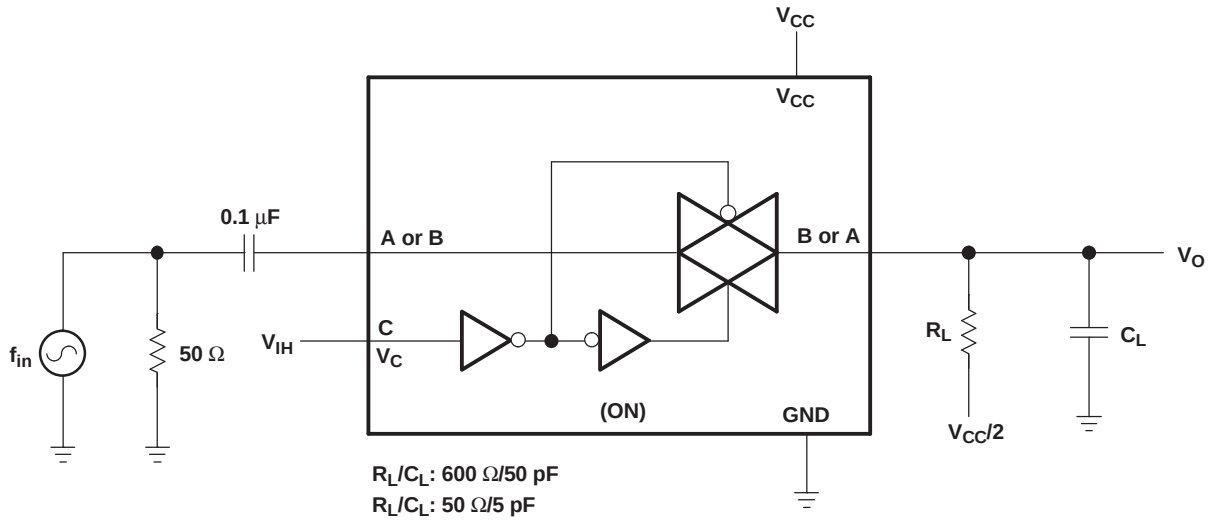



**Figure 6. Frequency Response (Switch ON)**

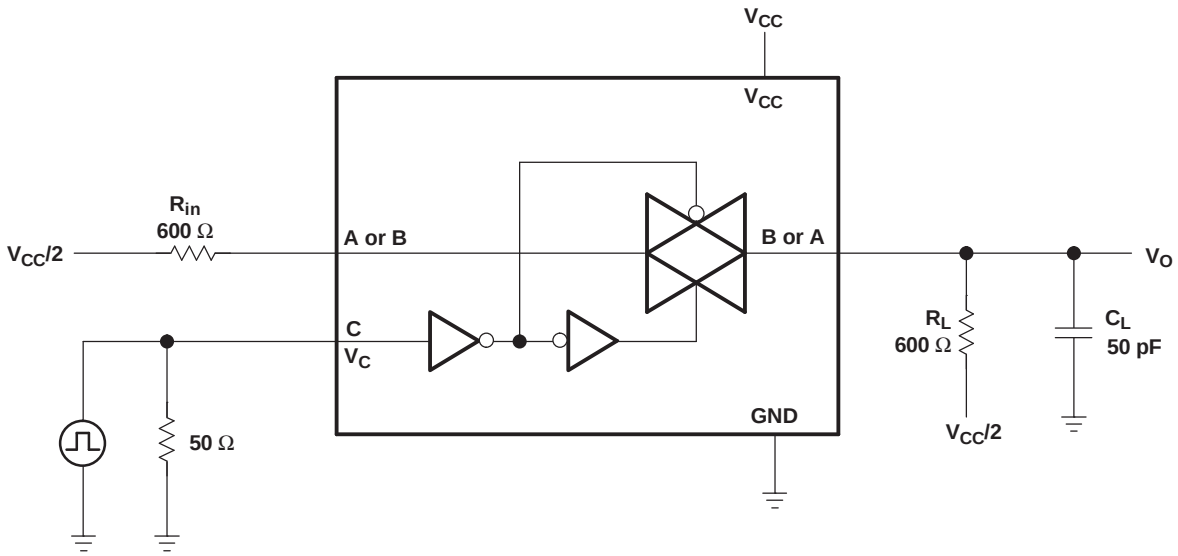



**Figure 7. Crosstalk (Control Input – Switch Output)**


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## PARAMETER MEASUREMENT INFORMATION

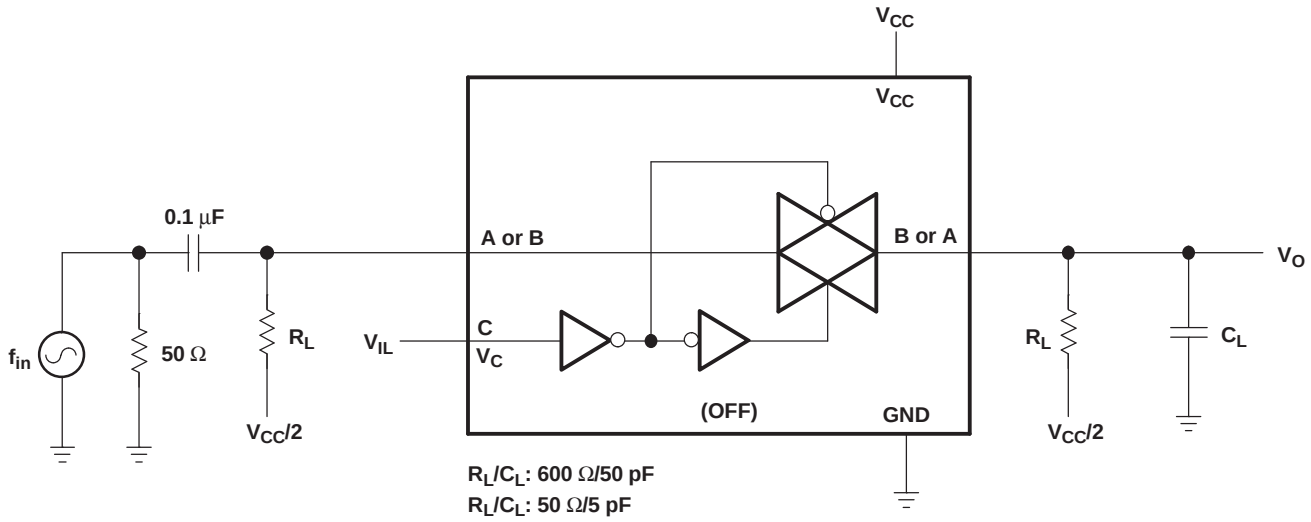



**Figure 8. Feedthrough (Switch OFF)**

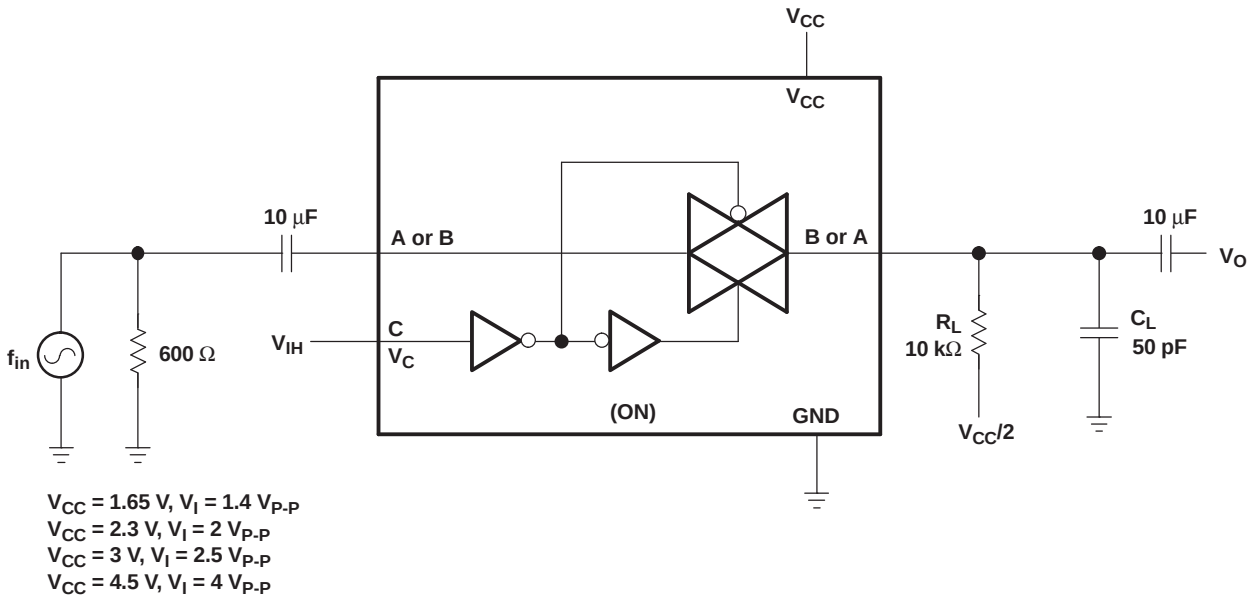



**Figure 9. Sine-Wave Distortion**

## REVISION HISTORY

| Changes from Revision L (January 2007) to Revision M | Page |
|---|---|
| • Added DSF and DRY packge to pin out graphic. | 1 |
| • Added Added DSF and DRY package to the ORDERING INFORMATION table. | 2 |

| Changes from Revision M (January 2012) to Revision N | Page |
|---|---|
| • Added Jumbo Reel to ORDERING INFORMATION TABLE. | 2 |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G66DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C662 ~ C665 ~ C66R ~ C66T) | Samples |
| SN74LVC1G66DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C662 ~ C665 ~ C66R ~ C66T) | Samples |
| SN74LVC1G66DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C662 ~ C665 ~ C66R ~ C66T) | Samples |
| SN74LVC1G66DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C665 ~ C66R) | Samples |
| SN74LVC1G66DBVTE4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C665 ~ C66R) | Samples |
| SN74LVC1G66DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C665 ~ C66R) | Samples |
| SN74LVC1G66DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65 ~ C6F ~ C6K ~ C6O ~ C6R ~ C6T) | Samples |
| SN74LVC1G66DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65 ~ C6F ~ C6K ~ C6O ~ C6R ~ C6T) | Samples |
| SN74LVC1G66DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65 ~ C6F ~ C6K ~ C6O ~ C6R ~ C6T) | Samples |
| SN74LVC1G66DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65 ~ C6R ~ C6T) | Samples |
| SN74LVC1G66DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65 ~ C6R ~ C6T) | Samples |
| SN74LVC1G66DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C65 ~ C6R ~ C6T) | Samples |
| SN74LVC1G66DRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C67 ~ C6R) | Samples |
| SN74LVC1G66DRLRG4 | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (C67 ~ C6R) | Samples |
| SN74LVC1G66DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C6 | Samples |
| SN74LVC1G66DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C6 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G66YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (C67 ~ C6N) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G66 :**

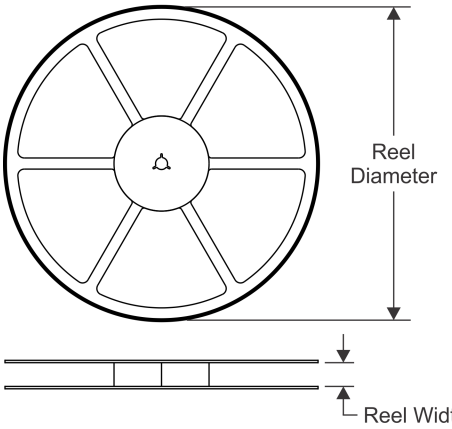
- Automotive: SN74LVC1G66-Q1

NOTE: Qualified Version Definitions:

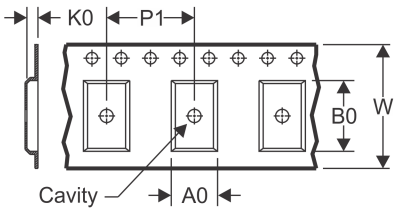
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

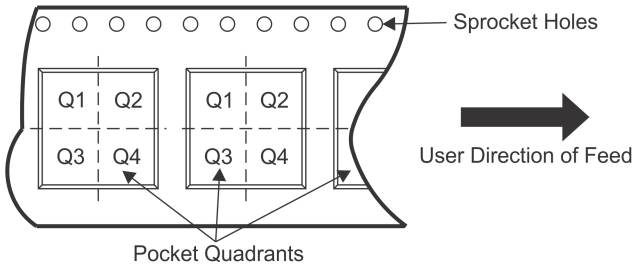



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

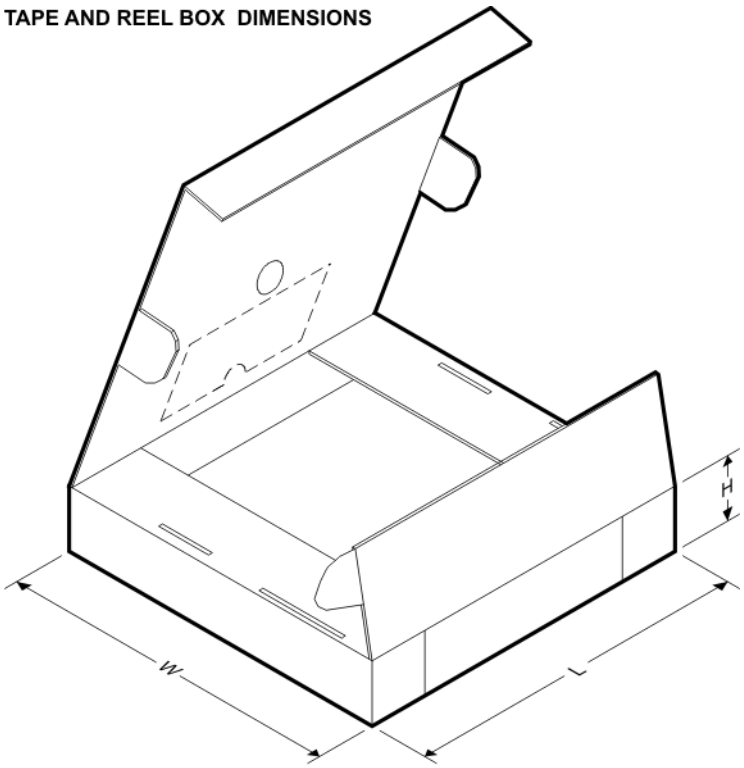
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.2 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.2 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DRLR | SOT | DRL | 5 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DRLR | SOT | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G66DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G66DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G66YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

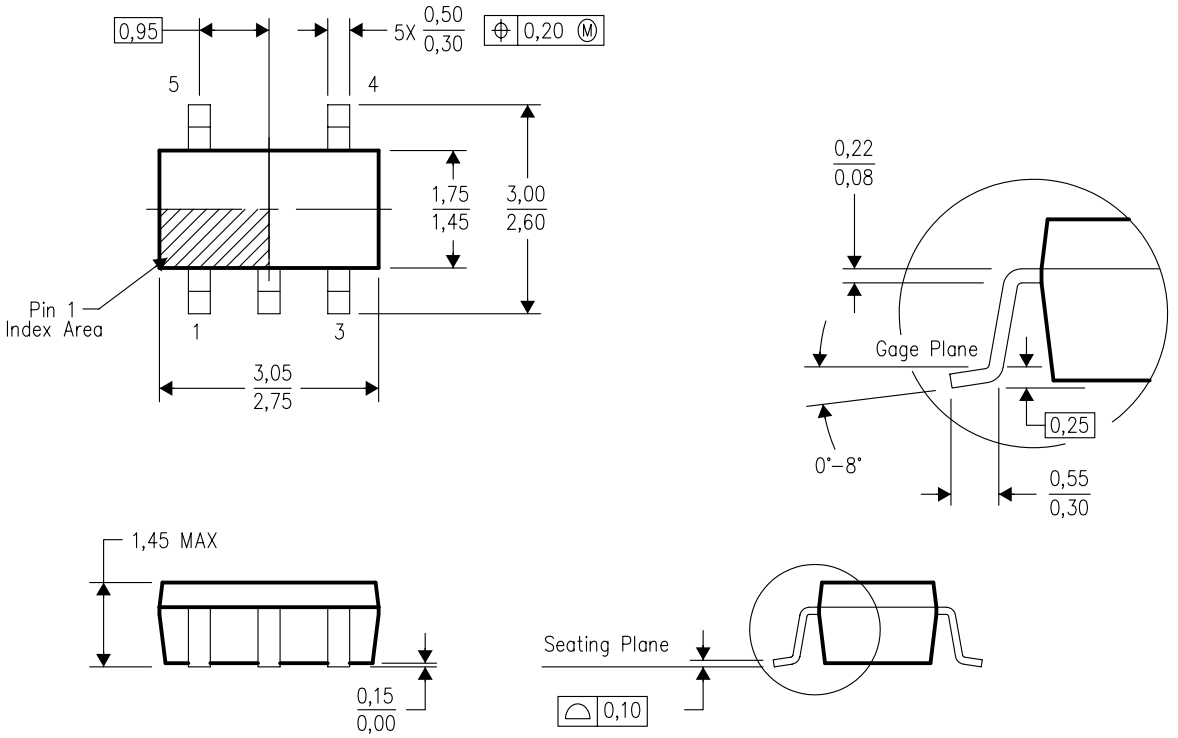
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G66DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DCKR | SC70 | DCK | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G66DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G66DRLR | SOT | DRL | 5 | 4000 | 180.0 | 180.0 | 30.0 |
| SN74LVC1G66DRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G66DRYR | SON | DRY | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74LVC1G66DSFR | SON | DSF | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74LVC1G66YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

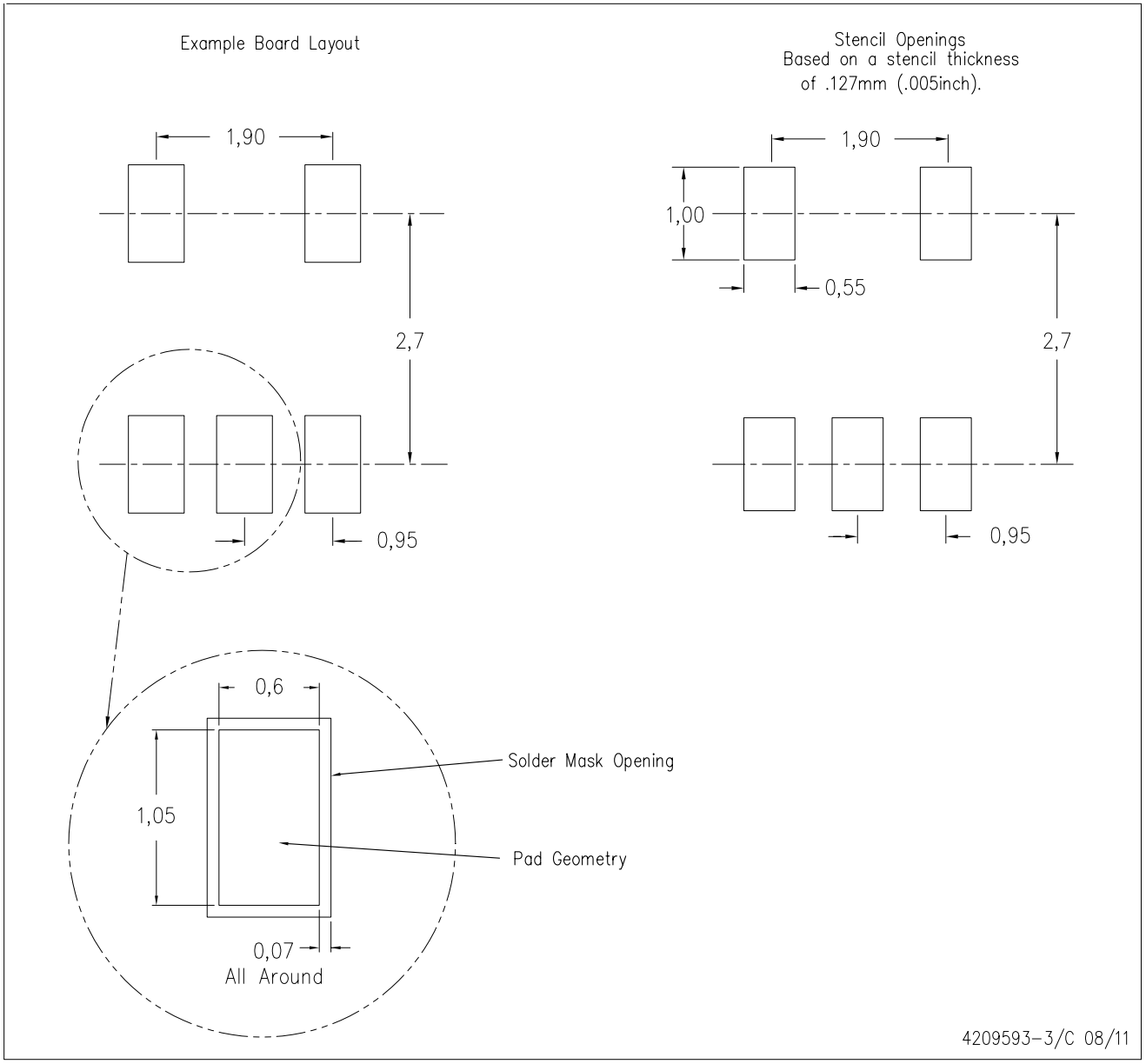
## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/K 03/2006

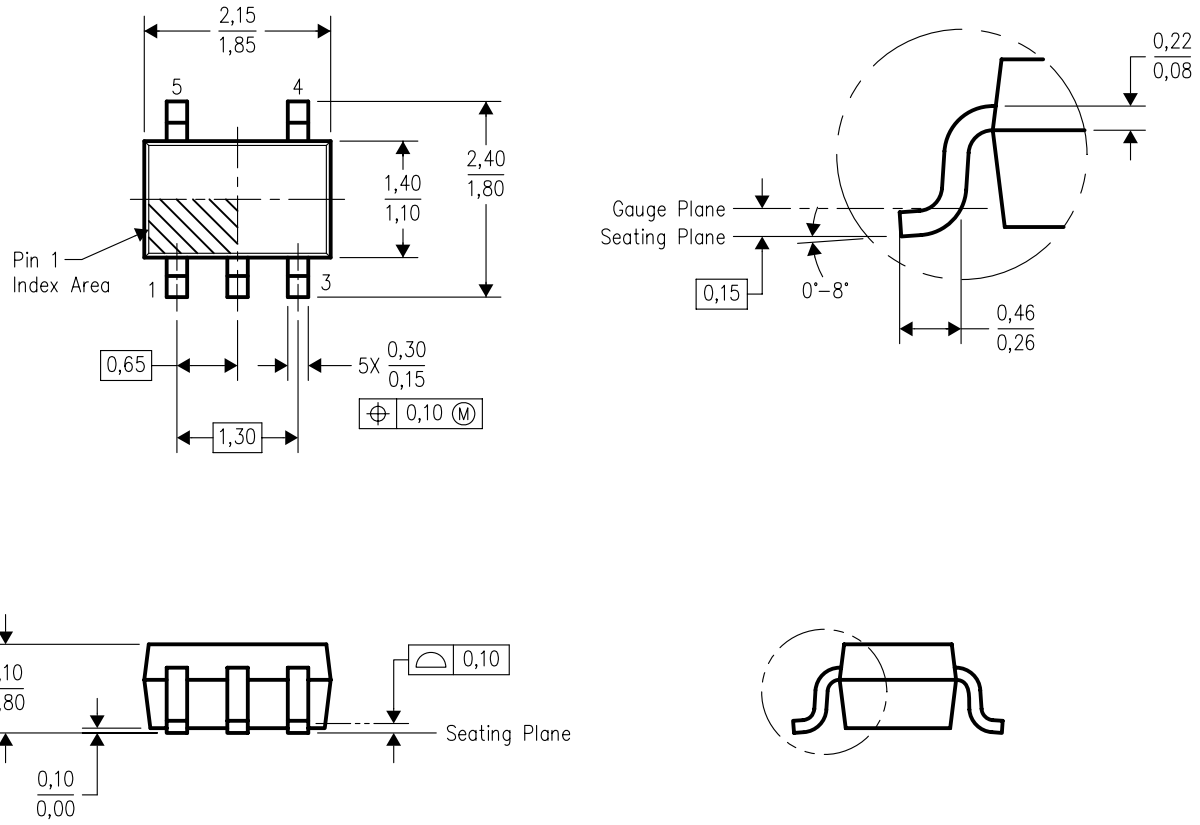
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

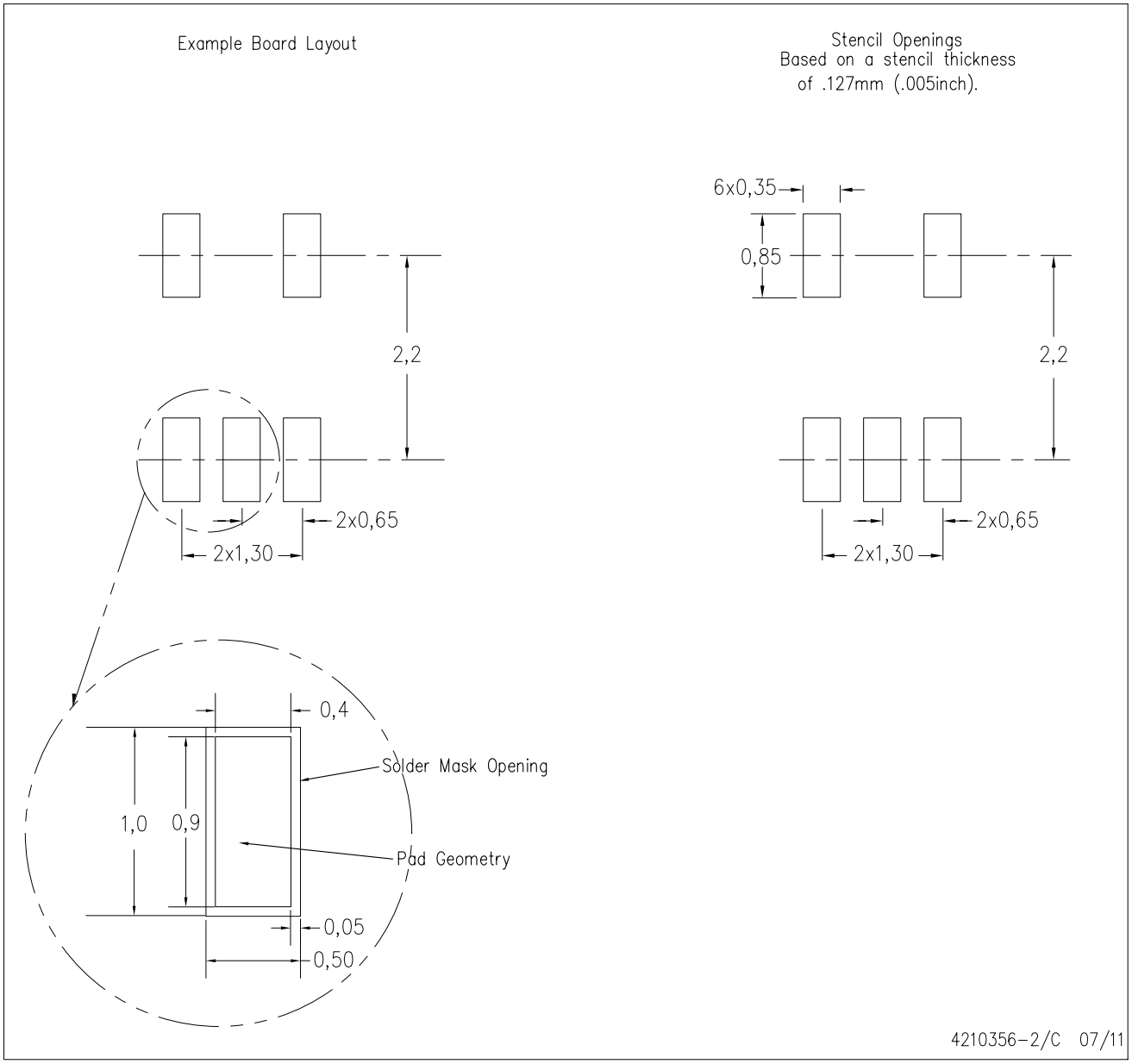
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



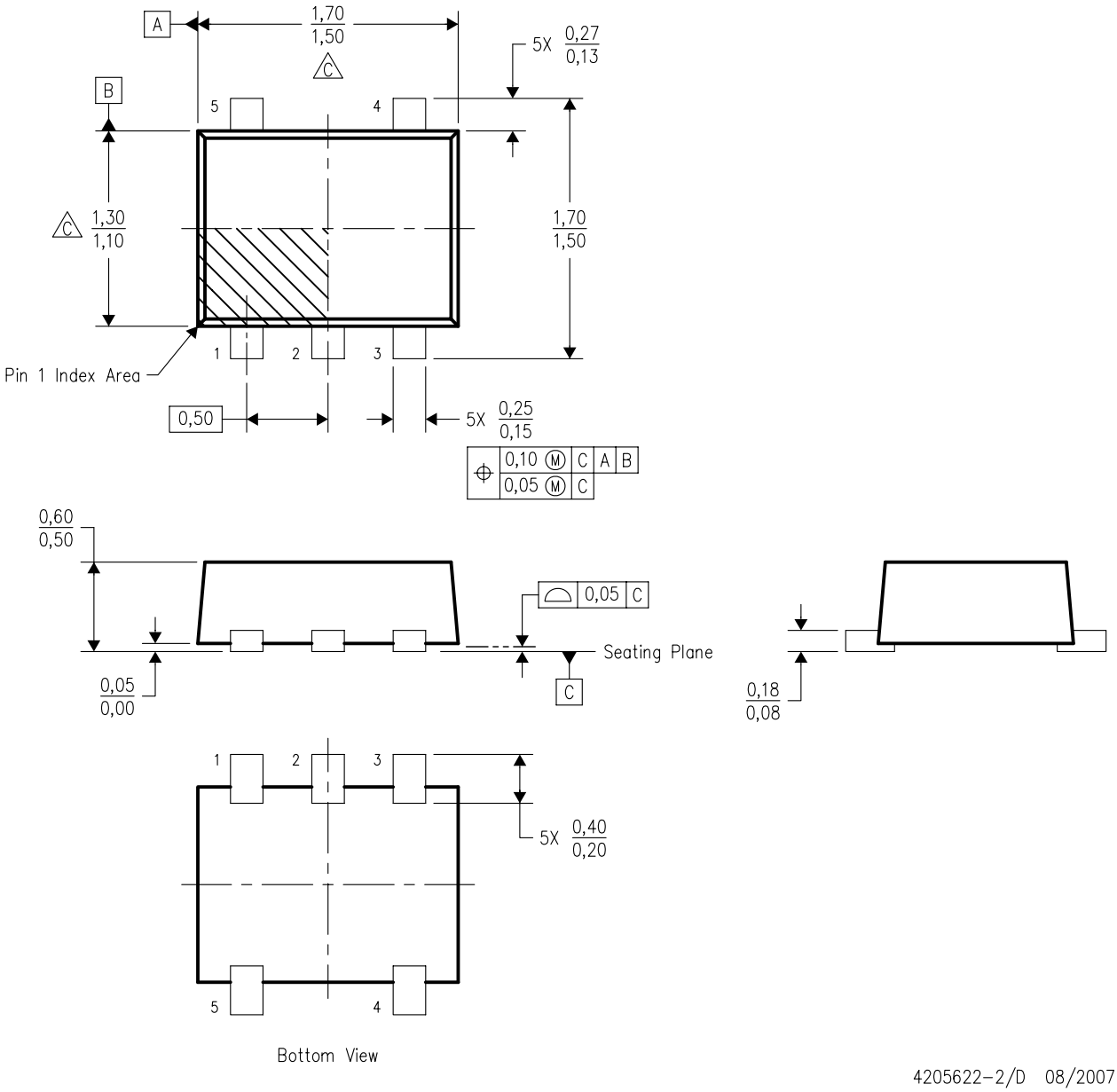

4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



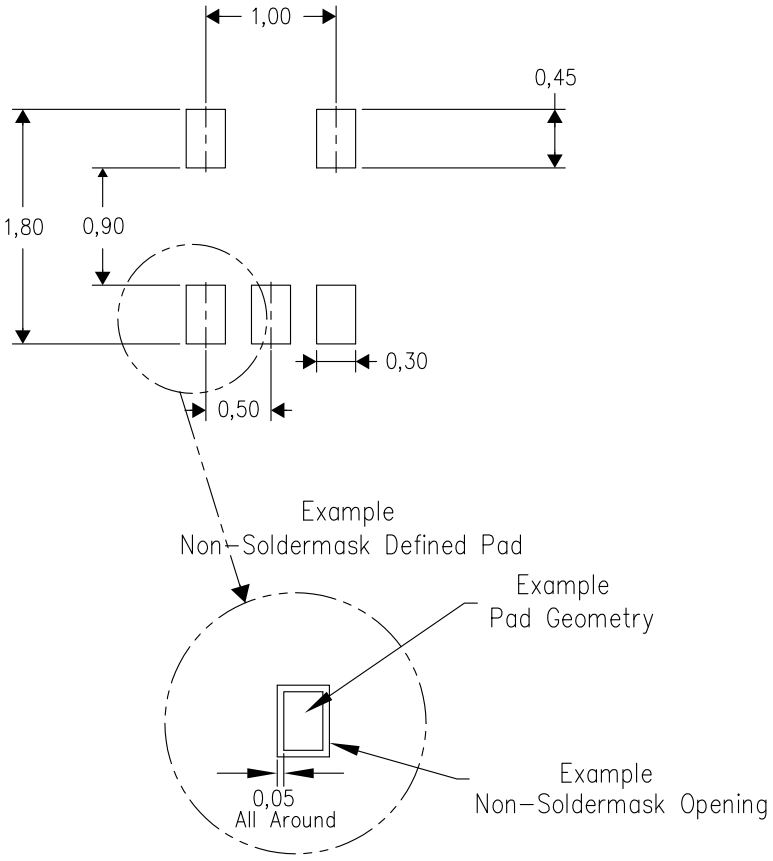

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



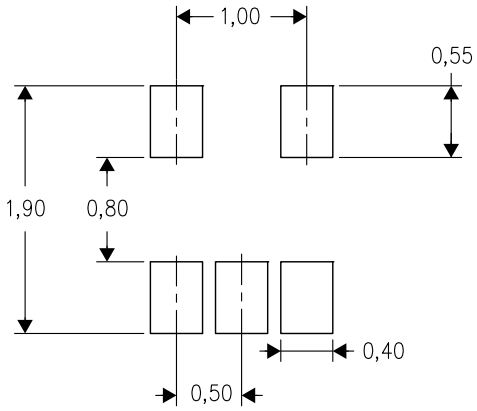

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



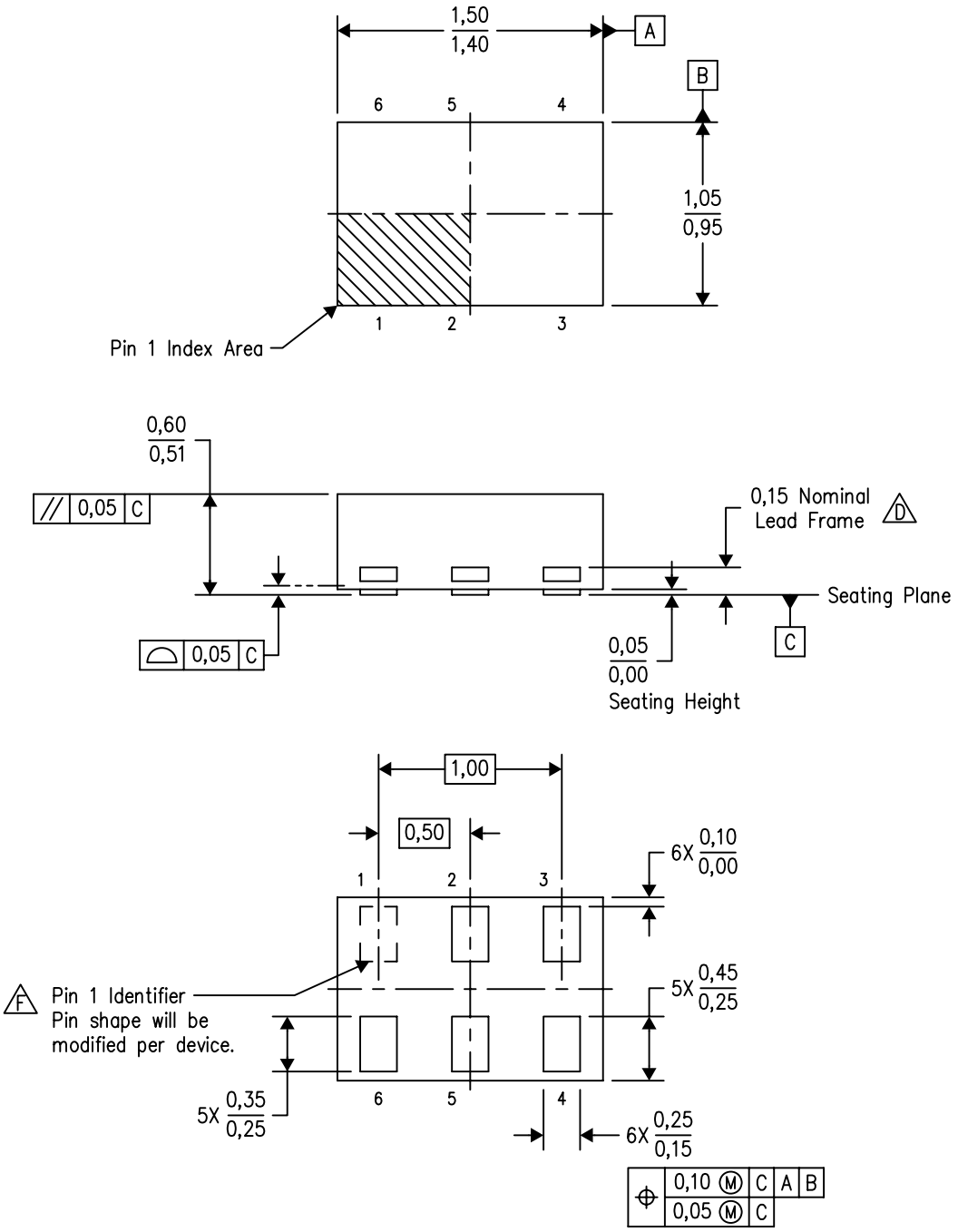

Example Stencil Design
(Note E)




4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

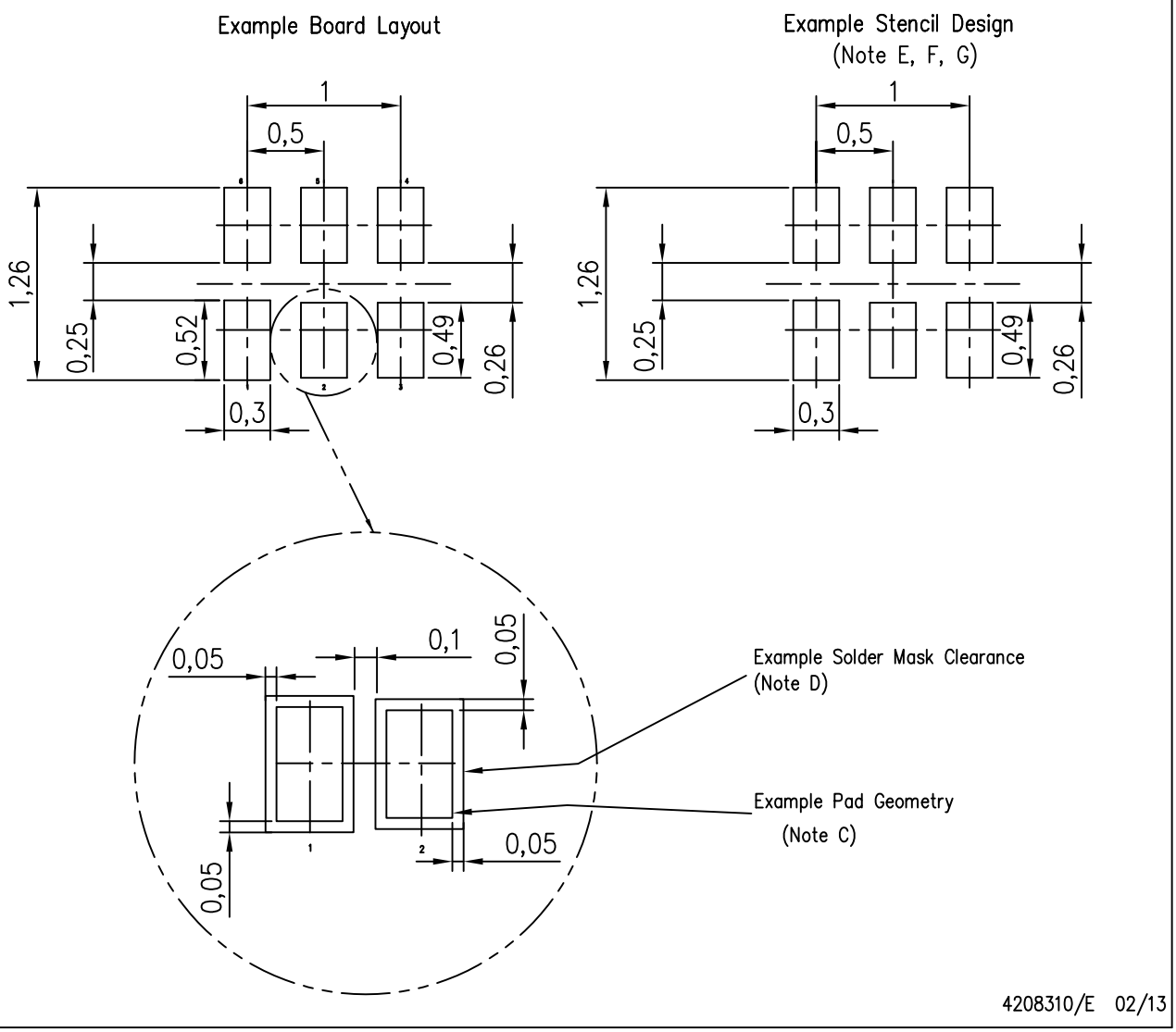
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4207181/F 12/11

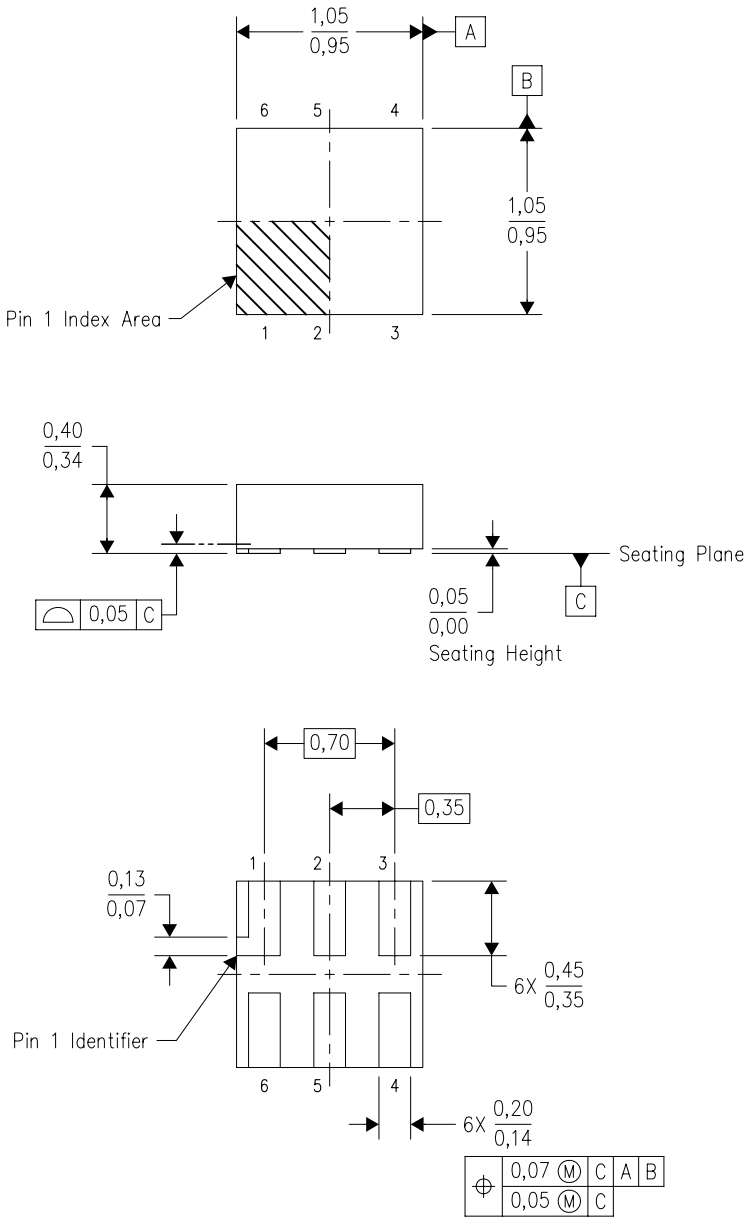
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

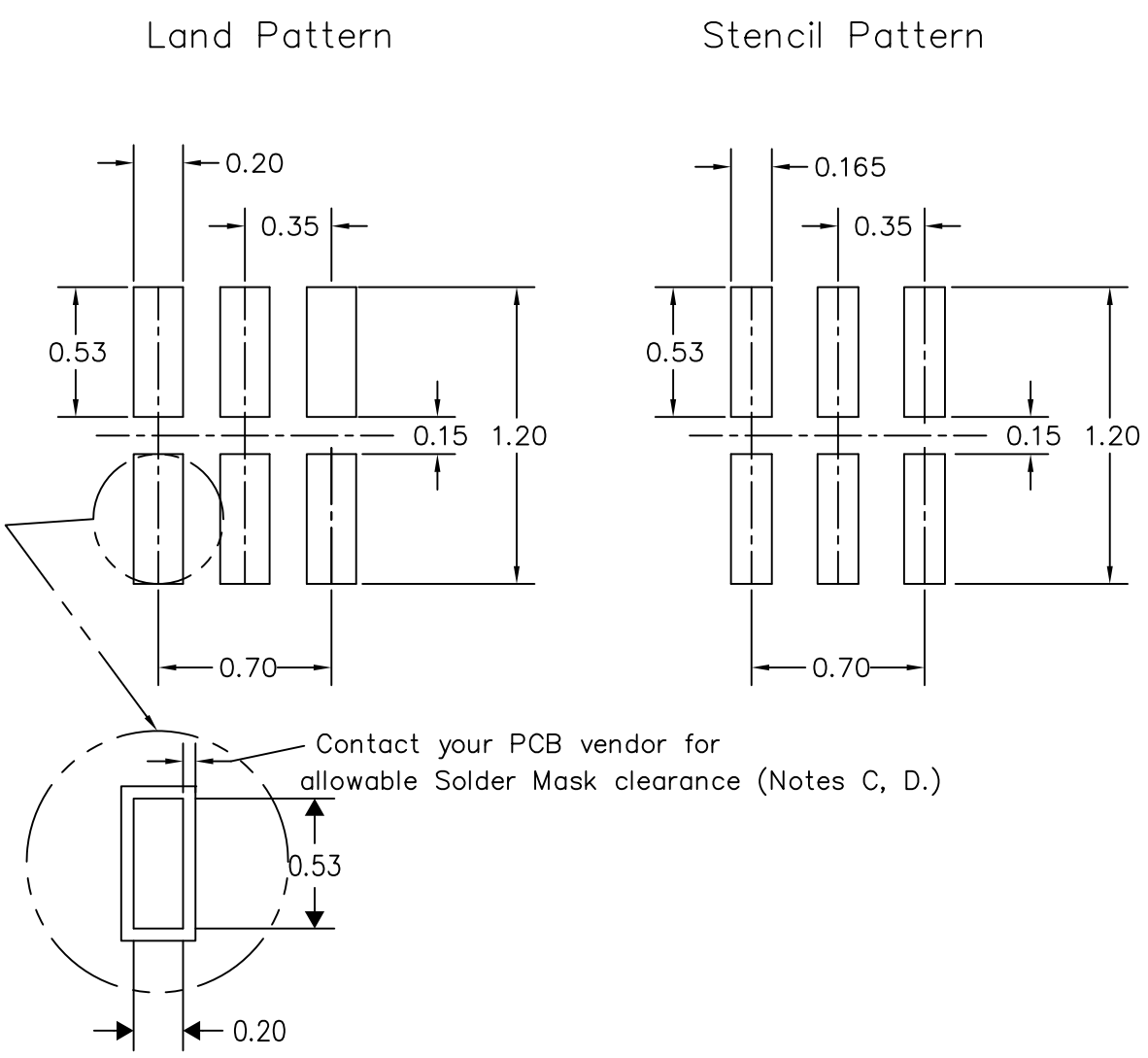
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4208186/E 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation X2AAF.

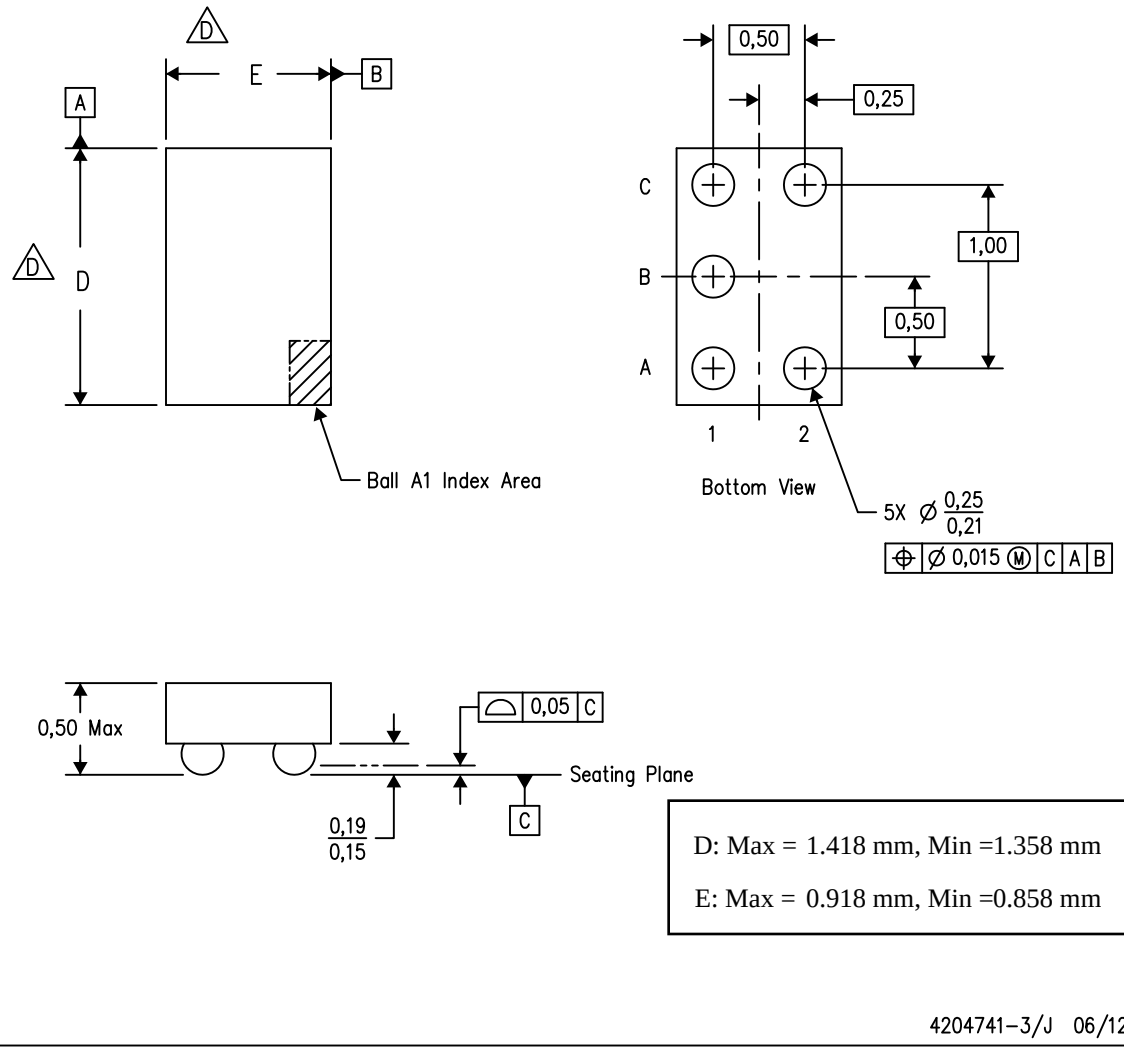
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4210277/D 05/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. This package is a Pb–free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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